Tips & Solution Seminar :

시뮬레이션 최신 동향 :

5 to 6Gen High Speed Interconnection

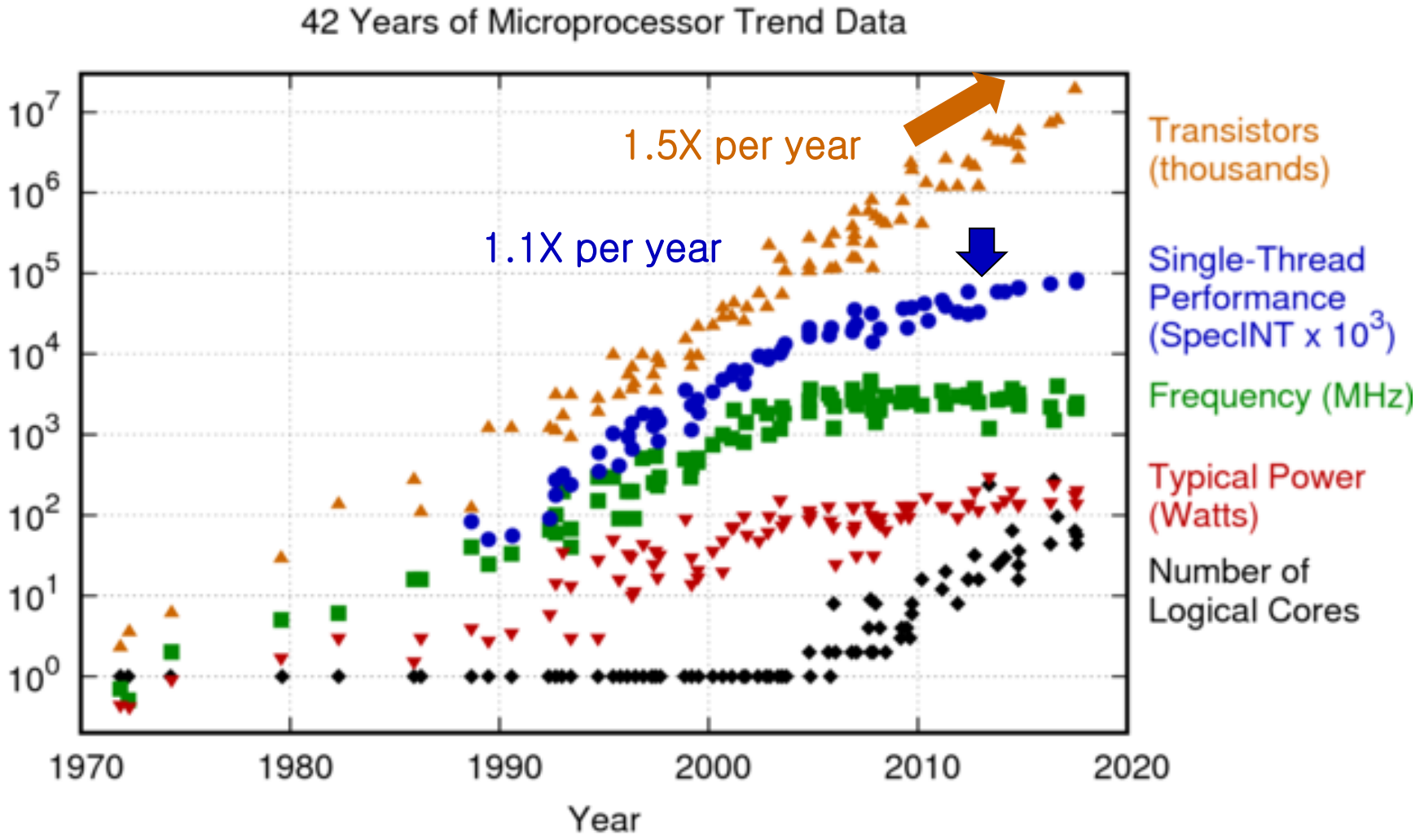
정성일, sijeung@huwin.co.kr , 010-3381-1417

2023. 6. 23

Contents :

5 to 6Gen High Speed Interconnection

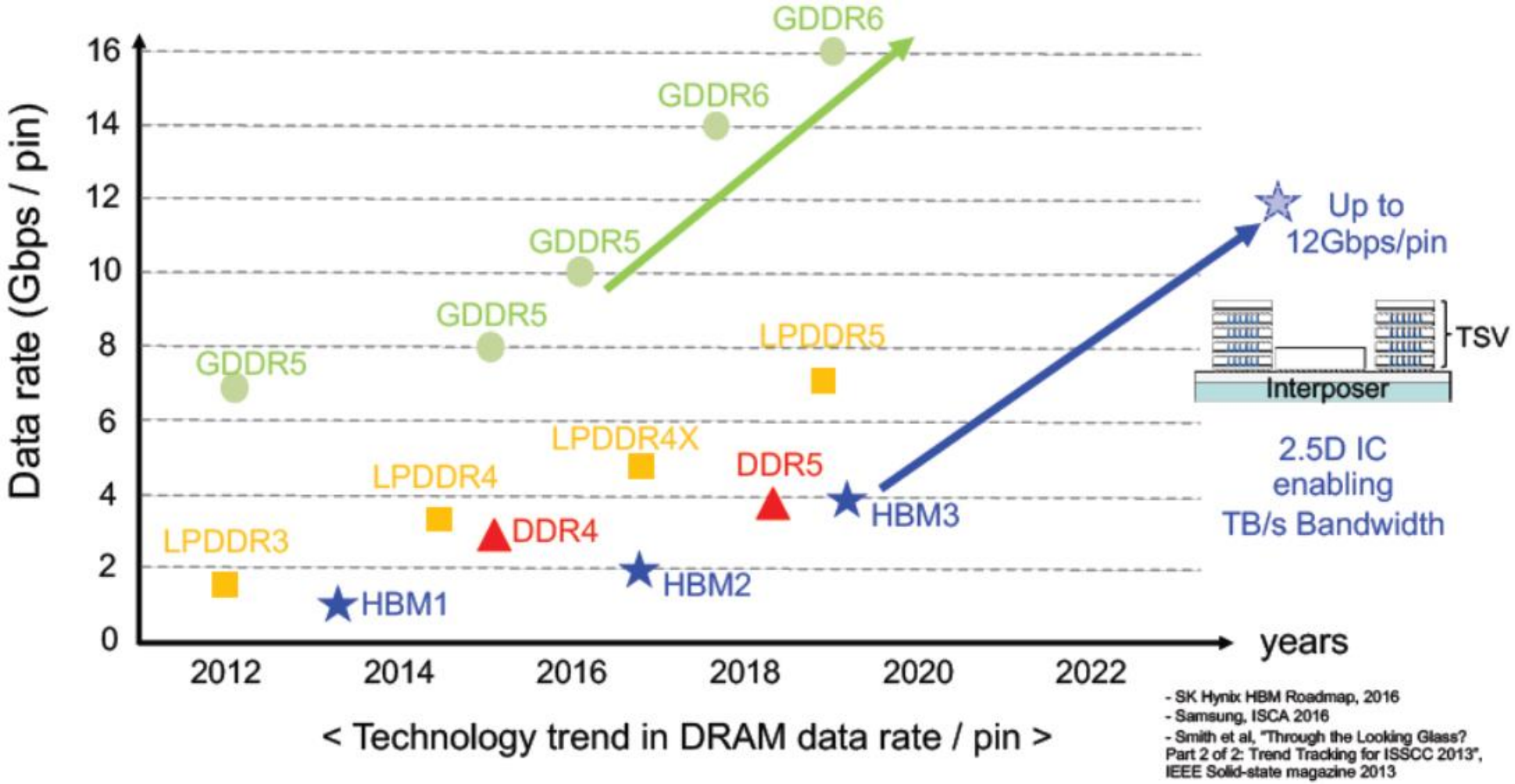
5 to 6Gen 동향 : Processor Trend



* Source : https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/

5 to 6Gen High Speed Interconnection

5 to 6Gen 동향 : DRAM Trend



< Technology trend in DRAM data rate / pin >

- SK Hynix HBM Roadmap, 2016
- Samsung, ISCA 2016
- Smith et al, "Through the Looking Glass? Part 2 of 2: Trend Tracking for ISSCC 2013", IEEE Solid-state magazine 2013

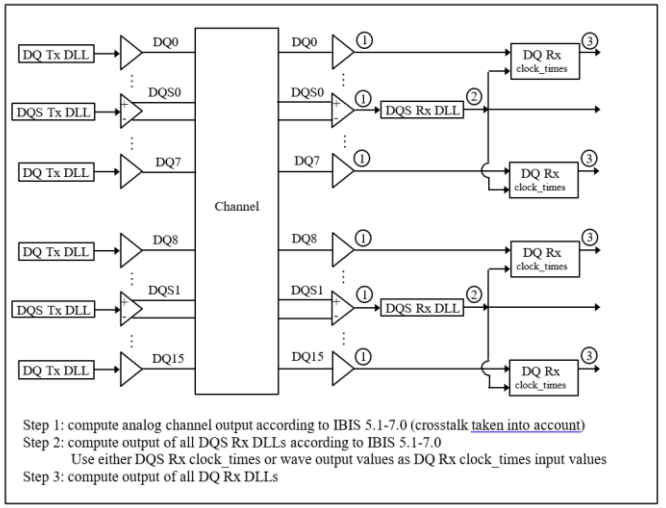
5 to 6Gen 동향 : DRAM Trend

DDR5 Progress

- IBIS 7.1 improves IBIS-AMI support for DDR5
  - AMI Reserved Parameter DC_Offset for inherent signal DC bias
  - C_comp Model for analog model improvement
  - GetWave Clock input for forwarded clocking (DQS)
  - AMI Reserved Parameters Component_Name and Signal_Name for DQ-level buffer model tuning
  - Backchannel Statistical Training
- EDA Tools
  - Capturing system non-linearities for Init and/or GetWave functions
  - DDR5-specific EDA tool support for IBIS-AMI model setup, bus analysis, sweeps, and validation

*Source : Designcon2022-SLIDES_Track2_Panel_AMI_Models_7yearItch_Telian2-1.pdf

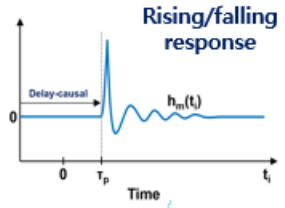
Rx DFE w DQS clocking

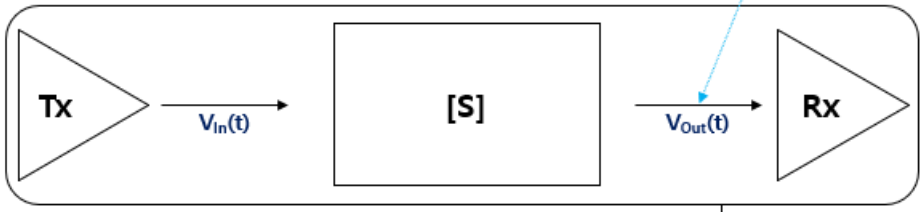


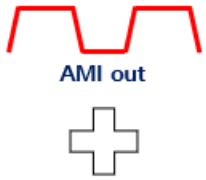
Parameter: DC_Offset
Required: ~~No, and illegal before~~ AMI_Version 7.1
Direction: Rx
Descriptors:
Usage: In
Type: Float
Format: Value
Default: <numeric_literal>
Description: <string>

Definition: The input value of DC_Offset is the mean value of the steady state high and low voltages of the analog channel step response at the Rx pad.

Usage Rules: If the impulse response was generated by differentiating the analog channel step response, then the input value of DC_Offset should be the same as the average of the step response initial and final voltages.





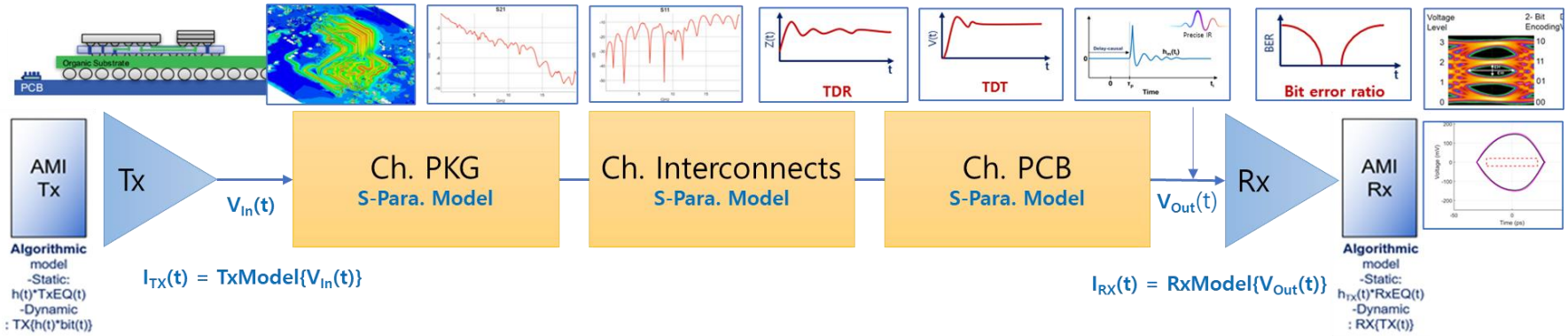


DC offset

The EDA tool ignores the DC_Offset value specified in the .ami file. It is the responsibility of the EDA tool to determine the input value of DC_Offset. The EDA tool may use any method to do this. The EDA tool may use the input value of DC_Offset to post process data returned by the AMI model to graphically compare the waveform output of Rx AMI_GetWave to the input waveform without the DC_Offset subtracted.

5 to 6Gen High Speed Interconnection

5 to 6Gen 동향 : High-Speed, High-density, High-power



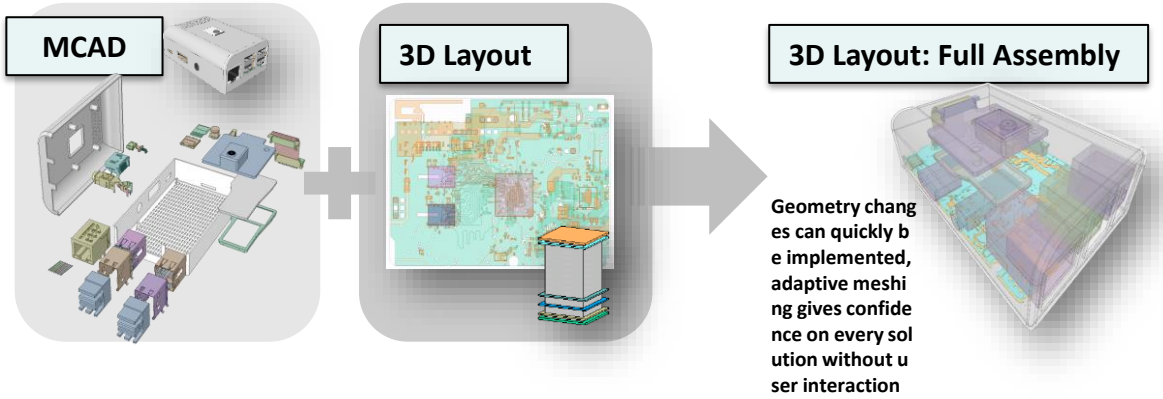
- Electronic System : High-speed, High-density, High-power
- 2023 : 800Gb(100G-PAM4 x 8lane) Ethernet , PCIe Gen6(PAM4), DDR5, GDDR6/7(PAM4)
- Copper Traces are lossy at high-speed
- Thermal Integrity
- Silicon Interposer (TSV)
- DC~80GHz S-parameters modeling
- Accurate Impulse response from S-parameters
- Large number of ports (signals) ch. Models -> ~10GB
- AMI model for estimating BER/Eye Eye-diagram

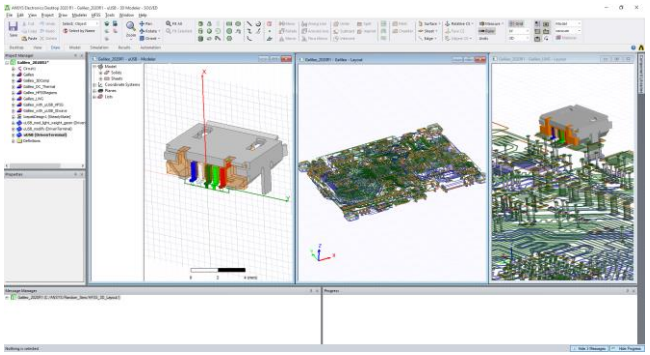
5 to 6Gen High Speed Interconnection

5 to 6Gen 동향 : High-Speed, High-density, High-power

Signal return through vias, PKG, wire-bonding, connector, cable :

- Non ideal Transmission Line region
- 3D EM coupling => 3D region (Standard : ANSYS HFSS) solving needed
- Loop resistance, Inductance on signal return (Common) path => X-talk, reflections
- Full X-talk transient solving and verification system needed
- Mixing CAD, Mixing Solvers needed





* Source : ANSYS

5 to 6Gen High Speed Interconnection

5 to 6Gen 동향 : Chiplet AI

네패스, 칩렛 이종 집적 초고성능 AI 반도체 개발 과제 '낙점'

서재창 기자 eled@hellot.net | 등록 2023.05.16 15:28:18 URL복사

[무료교육 마감임박] AI융합 제조산업 현장 빅데이터 디지털전환 전문인력 양성과정 (7월 진행)

사피온, 포항공대, 광주과학기술원(GIST) 등과 컨소시엄 구성해 개발 추진

네패스가 추진한 '칩렛 이종 집적 초고성능 AI 반도체 개발' 과제가 과학기술정통부 주관 국가공모에 선정됐다.

네패스가 총괄 및 1세부를 맡은 이번 사업은 AI 반도체 설계업체인 사피온, 포항공대, 광주과학기술원(GIST) 등과 컨소시엄을 구성해 개발을 추진하게 된다. 사피온이 AI용 NPU(Neural Processing Unit)를 개발하고, 다수의 소자를 네패스가 칩렛 패키지로 구현하는 프로젝트다.

* Source : https://www.hellot.net/news/article.html?no=78002

Huwin ACVS :

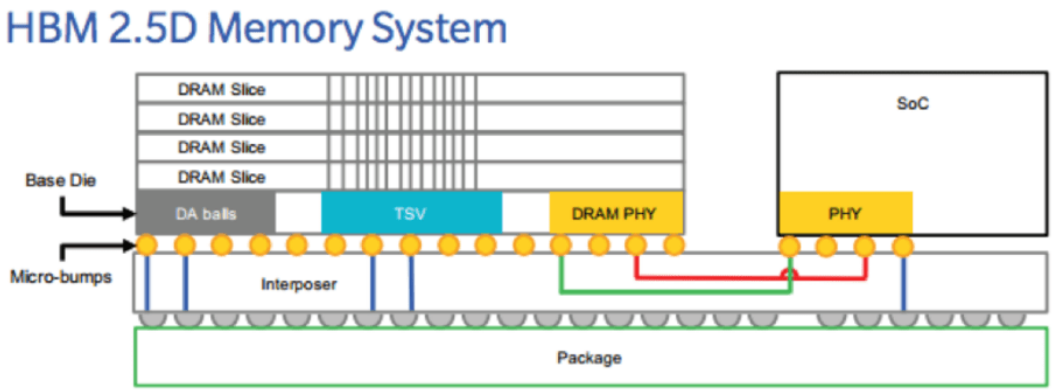
Advanced (AI) Chip Verification System

HBM3
UCIe
PCIe Gen6
EM (ANSYS) 해석 자동화
Eye-diagram 최적화 위한 Tx/Rx 모델

5 to 6Gen 동향 : HBM

High Bandwidth Memory (HBM) DRAM 표준 :

- GDDR보다 더 높은 메모리 대역폭을 달성하기 위해 적층 형태로 설계.
- 2013년 SK Hynix에서 최초로 HBM chip 생산, JEDEC 표준으로 채택됨.
- 2016년 HBM2 JEDEC 표준, 8 dies per stack, 2GT/s, 256GB/s per package
- 2019년 HBM2E, 8 dies per stack, 3.6GT/s, 460GB/s per stack
- 2022년 HBM3 JEDEC 표준 238A, 12 dies per stack, 6.4GT/s, 819GB/s per stack

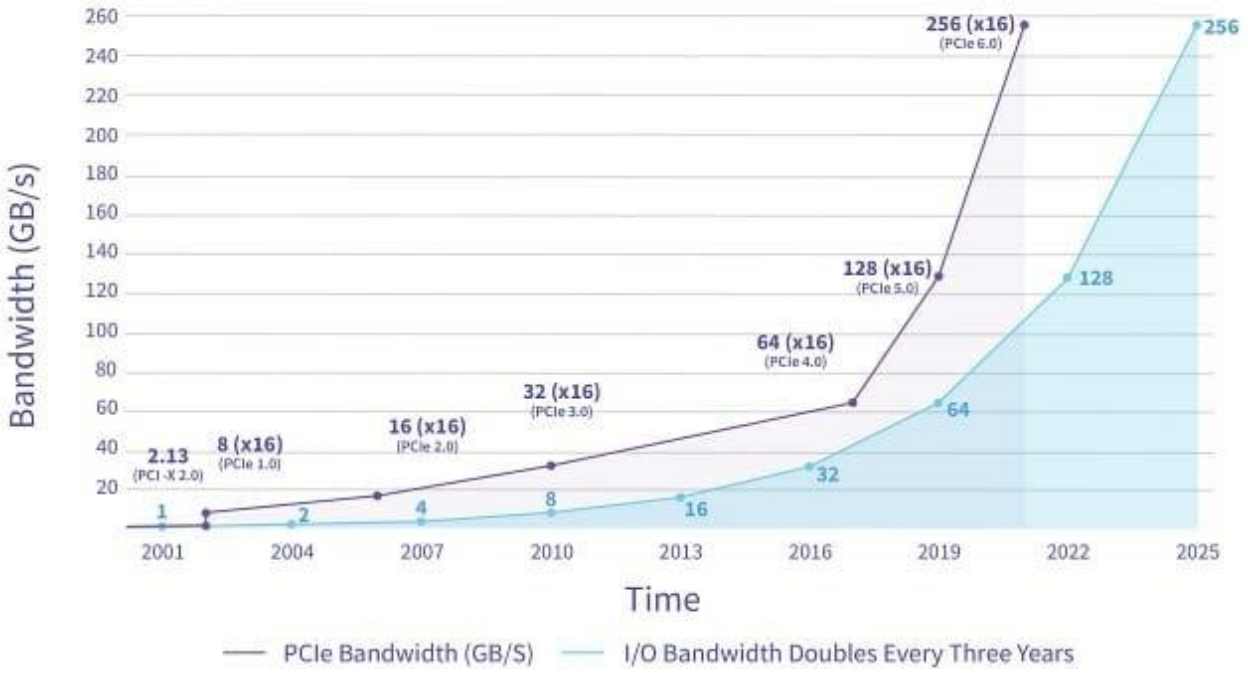


HBM 집적 패키지 (*Source : Rambus)

5 to 6Gen 동향 : PCIe

PCIe (Peripheral Component Interconnect Express) 표준 :

- 2022년 PCIe Gen6.0 규격 최종안 확정, 64GT/s, x16 lanes 로 구성, 최대 256GB/s 전송이며,
- PCIe Gen5 (32GT/s) 대비 PAM4 시그널링을 적용하여 데이터 대역폭을 확장함.



PCIe 규격 및 전송속도/대역폭 (*사진 = PCI-SIG)

5 to 6Gen 동향 : UCIe

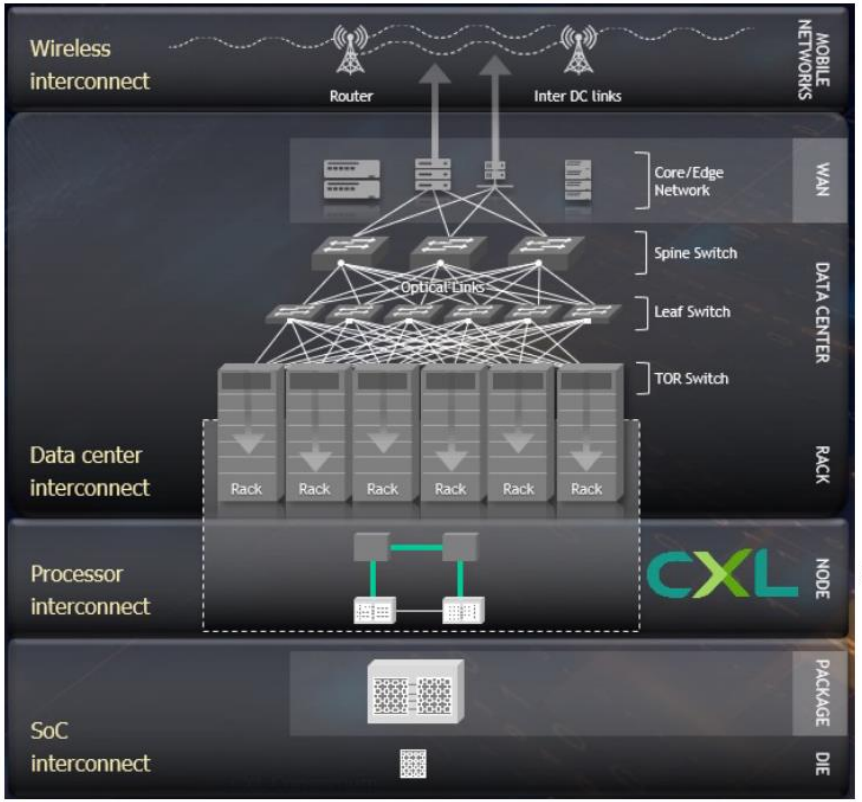
UCIe (Universal Chiplet Interconnect Express) 표준 :

- Rev. 1.0 (Feb. 2022)
- Die-to-die 패키지 레벨 통합을 위한 칩렛 인터페이스 표준
- PCIe Gen5/6, CXL 2/3 support
- Intel, AMD, Samsung, SK hynix, LG, Nepes, TSMC, NVIDIA, Qualcomm 등 major chipmaker 들 뿐 아니라, package, Interface IP 및 EDA 업체들이 대부분 참여하고 있음.
- Pitch 가 작아서 접합 오류 발생 가능성 높은 Advanced Package 설계에 대해 Interconnect Redundancy Remapping 에 대해 정의하고 있음.

5 to 6Gen 동향 : CXL

Introducing CXL

- **Processor Interconnect:**
  - Open industry standard
  - High-bandwidth, low-latency
  - Coherent interface
  - Leverages PCI Express® architecture
  - Targets high-performance computational workloads
    - *Artificial Intelligence*
    - *Machine Learning*
    - *HPC*
    - *Comms*



A new class of interconnect for device connectivity

*Source : Designcon2022- CXL_PCI-SIG_DesignCon 2022 Panel_03302022[80] - Read-Only.pdf

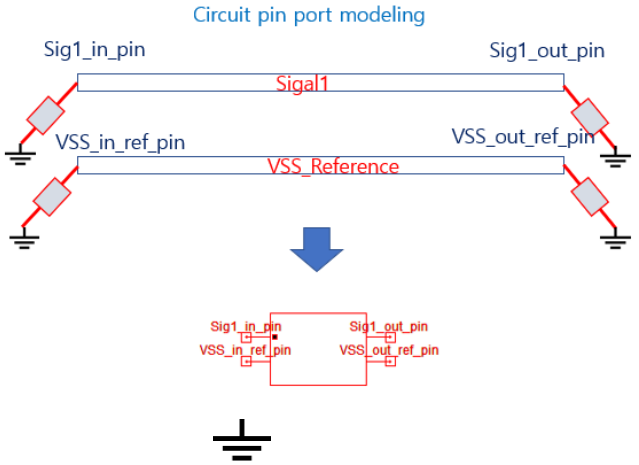
Contents :

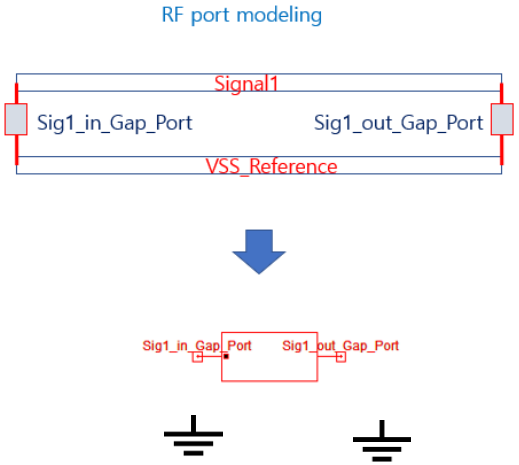
5 to 6Gen High Speed Interconnection

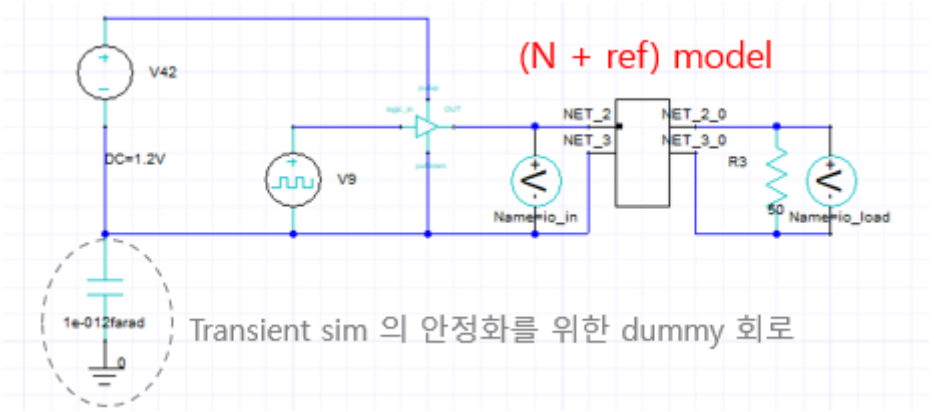
5 to 6Gen Tech. Issues :

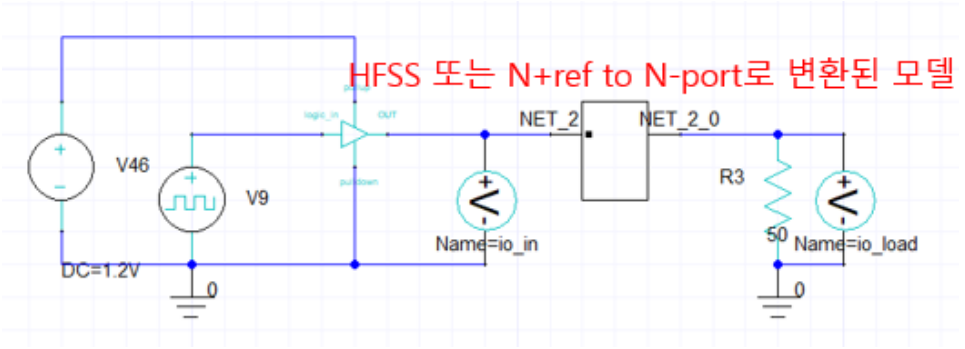
Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification







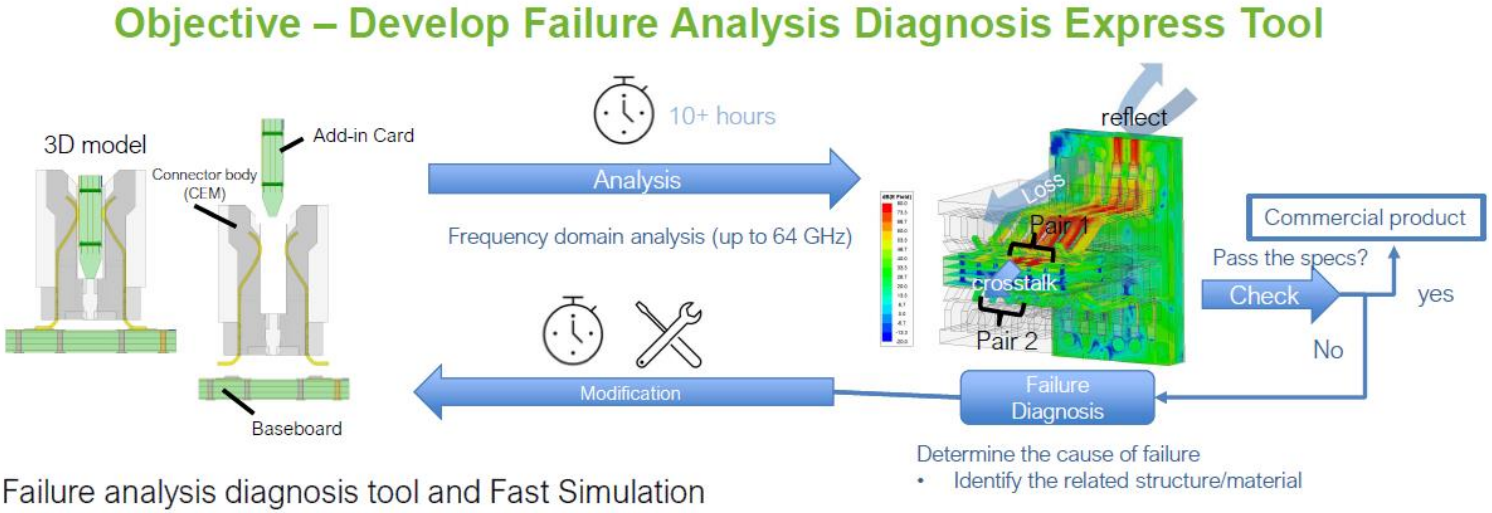


5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification



Failure analysis diagnosis tool and Fast Simulation

- Analysis: insertion loss, return loss, crosstalk, and impedances
- FEM 3D simulation: 3D electromagnetic simulation for high-frequency electronic products (e.g, Ansys HFSS)
  - High accuracy by solving wave equations in small mesh areas
  - Long design cycle: require finer mesh for devices at high-frequency (smaller wavelength) → need hours of simulation per design iteration
- Proposed 1D distributed physical based circuit model as an alternative and complementary express tool
  - Goal: accurately predict electrical performances and identify the failure mechanism (root causes of SI degradations)

* Source : SLIDES_Track 13_Distributed-Physical-Based_Transmission-Line Model_of_PCIe5 _He.pdf , DesignCon 2023

=> EM modeling 해석 시간, 효율 문제

➔ ANSYS SIwave Hybrid region

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

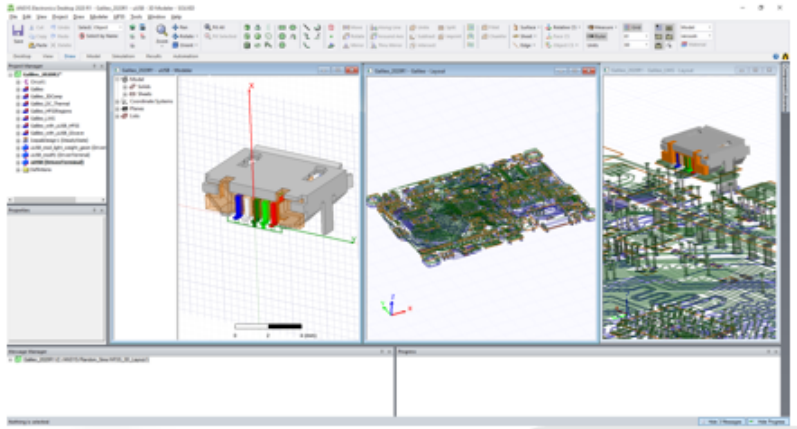
Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Signal Integrity

Mixing CAD

- Networking hardware will have to work with next generation signal rates of 28 and 56 Gbps to handle data loads of 49 exabytes per month by 2021. This will require data lanes to be modeled using a more holistic approach versus the piecemeal approach used in the past. Hence more complex geometries will need to be analyzed together.
- Ansys HFSS 3D (MCAD) – Use for modeling complicated 3D objects such as connectors, vehicles, complicated antennas, and other MCAD objects
- Ansys HFSS 3D Layout (ECAD) – Used for modeling circuit boards, chip packages, and chips. The ECAD environment is much easier to work with when simulating these types of objects.
- The ECAD and MCAD environments can be mixed using layout-driven assembly. In this case, 3D CAD models can be pulled into the ECAD environment and placed on or around circuit boards, etc.



* Source : ANSYS

=> Mixing CAD, Mesh Fusion, 3D Components

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

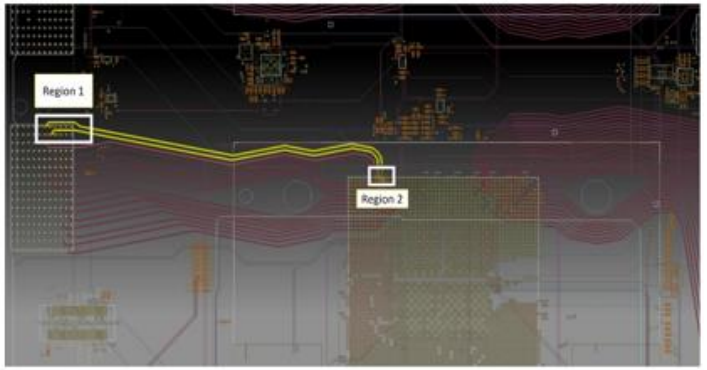
Tech. Issues :

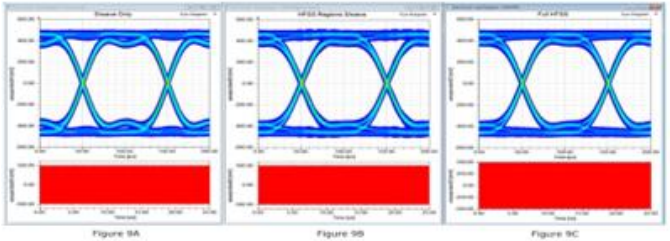
- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Signal Integrity

Mixing Solvers

- Design and analysis time reduction through mixing 2.5D and 3D Full-wave field solvers
- Ansys HFSS tackles complex geometries, such as exit routing under a BGA or connector landing patterns
- Ansys SIwave handles high-speed signal trace geometries





Simulation	Time
SIwave Only	10 hours and 39 minutes
SIwave with HFSS Regions	12 hours and 25 minutes
HFSS Only	30 hours and 39 minutes

Eye Characteristics	SIwave Only Simulation	HFSS Regions in SIwave Simulation	Simulation of the Cut Out in HFSS Only
Peak to Peak Jitter	6.6 ps	7.0 ps	7.0 ps
Minimum Eye Height	663.7323 mV	696.2321 mV	699.0568 mV
Minimum Eye Width	94 ps	93.6 ps	93.6 ps

* Source : ANSYS

=> Mixing Solvers : 2.5D (Fast SIwave) and 3D Full-wave (HFSS region)

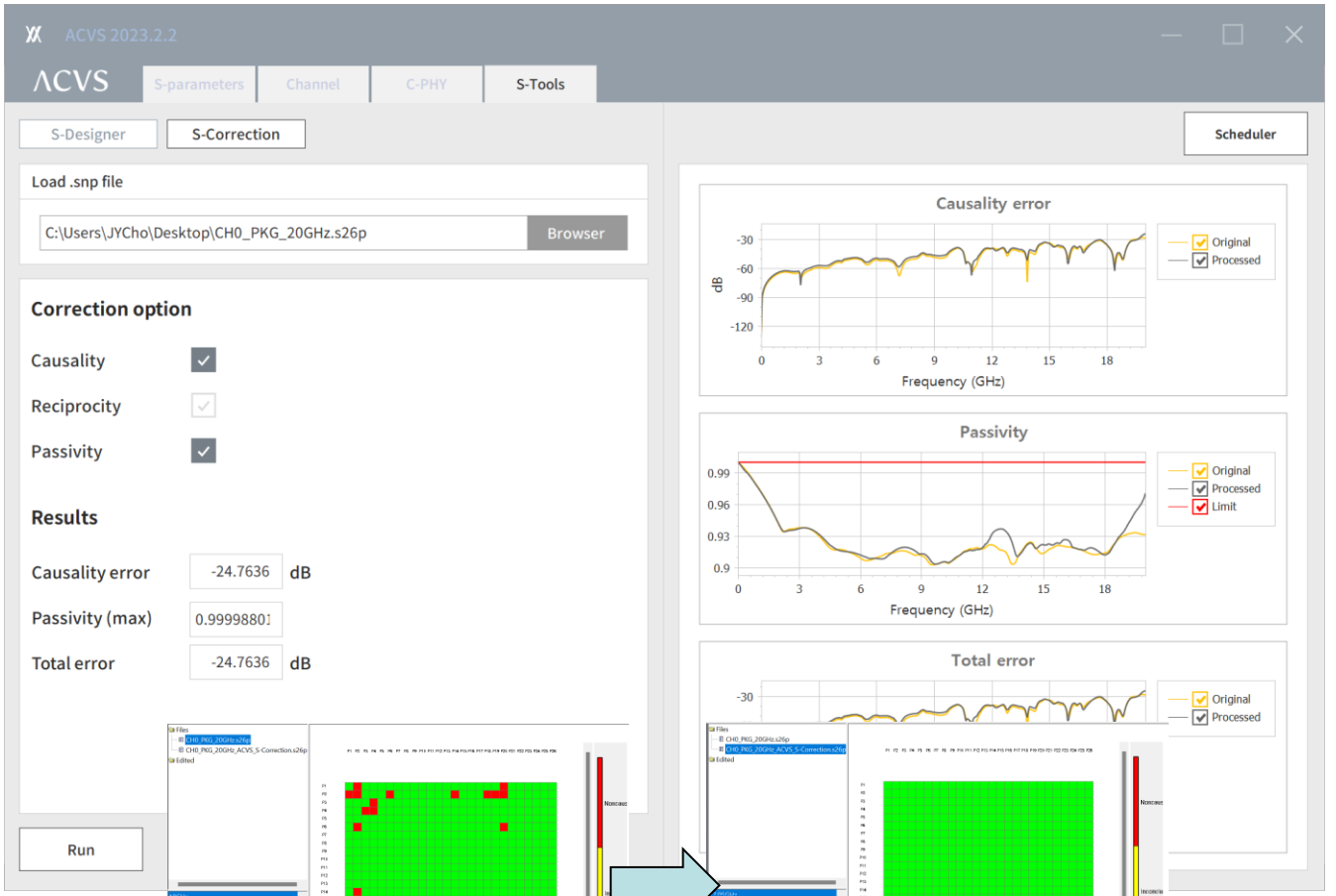
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Huwin S-tools : S-Correction => **Causality/Passivity enforcing**

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification



적용 전

➢ Non-causal error

적용 후

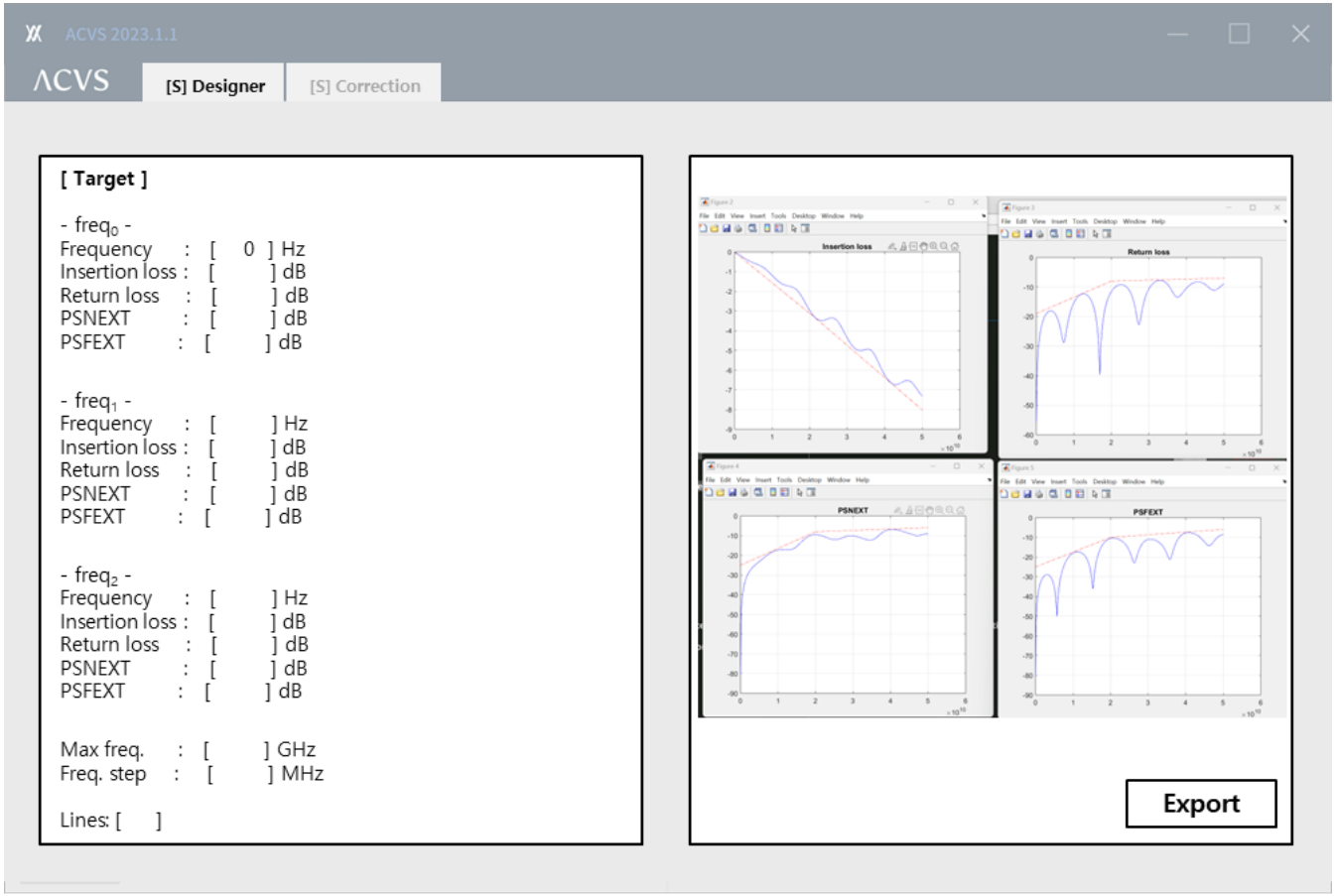
➢ Causal 확인

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Huwin S-tools : S-Designer => **channel .snp file generation**



UI concept

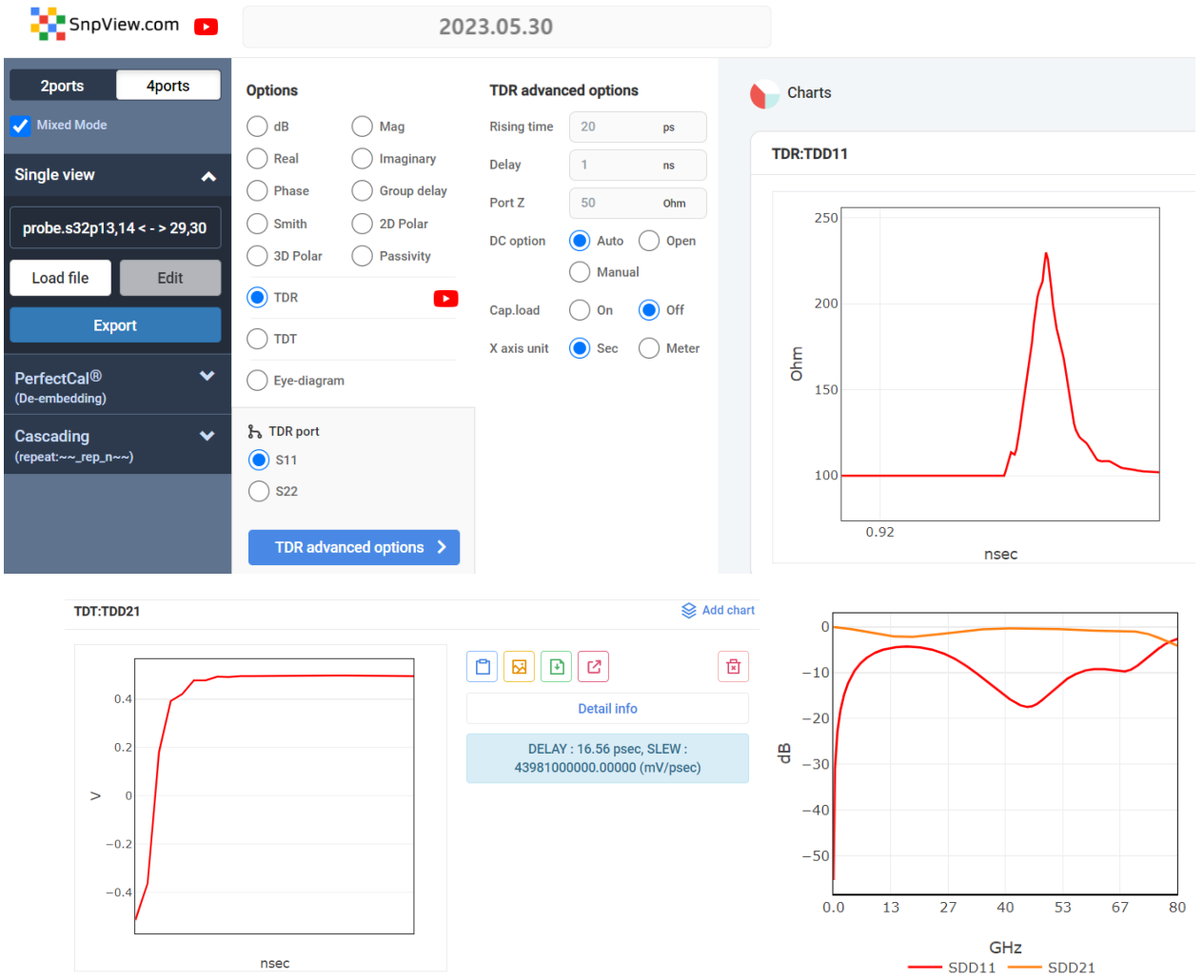
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Huwin www.snpview.com => **channel .snp file verification**



Accurate TDR/TDT , IL, RL

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Accurate impulse response

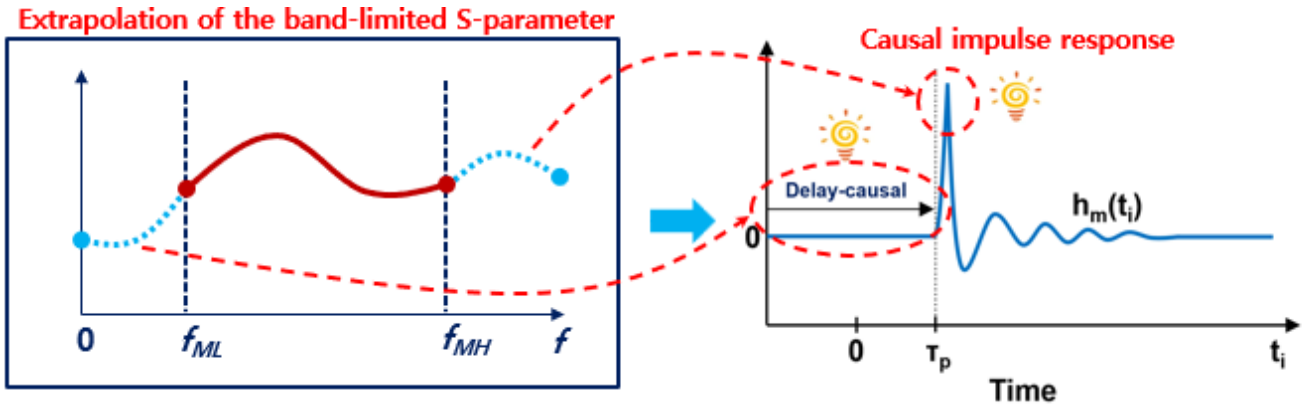
Correct adaptation of EQ in AMI simulation

Accurate results of AMI analysis

Huwin SimX engine

Extrapolation method for extracting accurate and causal impulse responses

- Low/high frequency range extension for the band-limited S-parameter
- Ensuring low-frequency accuracy and causality of the impulse response



5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

➢ Jitter Noise Analysis using ACVS :

✓ **ACVS Basic SI report to estimate the Jitter Noise**

=> Insertion Loss/ Return Loss /X-talk Summation

=> Accurate TDR/TDT report

=> Quick report for the jitter noise estimation in early design stage

✓ **ACVS Eye/BER report to estimate the Jitter Noise**

=> Accurate Eye/BER report to measure

- DJ (deterministic jitter), Non intrinsic (design-related deviations) jitter which can be controlled or fixed with appropriate signal Ch. design improvements.

- Periodic modulation (phase, amplitude, and frequency), Duty cycle distortion(DCD), Inter-symbol interference (ISI), Crosstalk, Reflection caused by unmatched media

=> ACVS has the function of Fast Eye (Hawk eye) diagram/BER including DDJ, ISI, Distortion, Crosstalk, Reflections through Ch.

=> Faster solution with highest accuracy

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

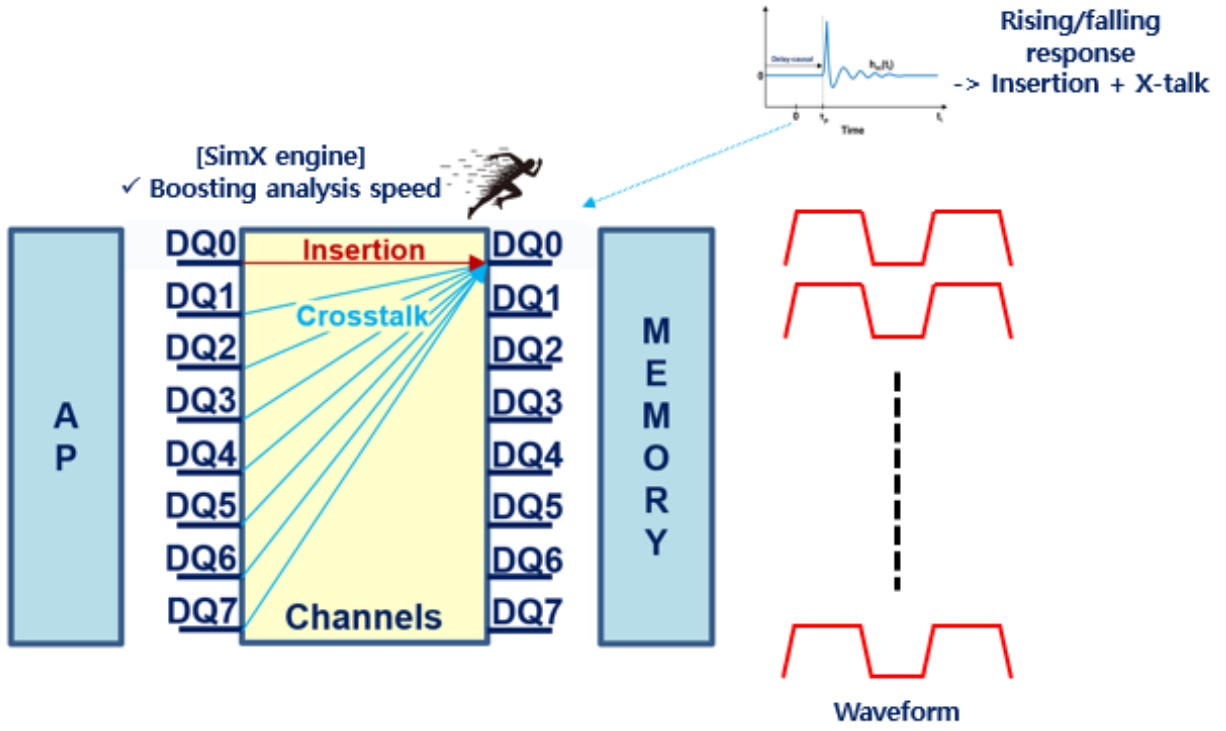
- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Huwin Memory module: Single-ended AMI (DDR5/GDDR6)

Next wave for SI/PI

Basic principle

- ➢ Extracing **All X-talk** responses
- ➢ Wave synthesis using all X-talk responses
- ✓ Computational load ↑



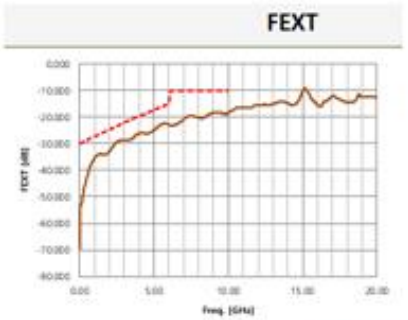
5 to 6Gen High Speed Interconnection

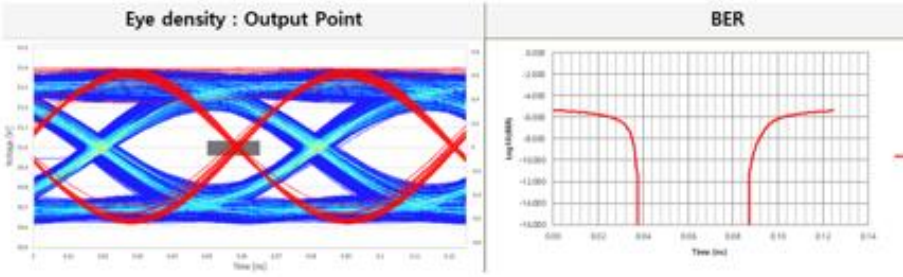
5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

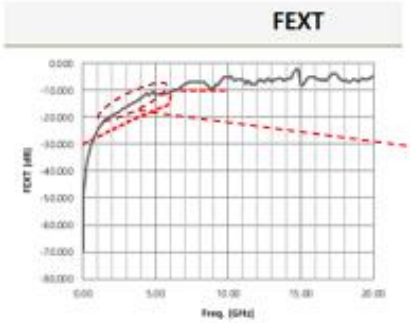
➢ Huwin ACVS Basic SI (FEXT) and Eye/BER report results correlation example for Jitter analysis

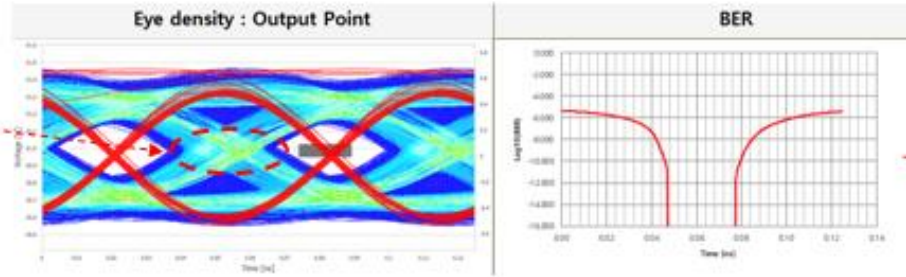




ACVS Basic report example of Good ch, Satisfy the FEXT limit (far end cross-talk summation)

ACVS EYE/BER report example of Good ch, With less Jitter noise





ACVS Basic report example of Bad ch, Over the FEXT limit (far end cross-talk summation)

ACVS EYE/BER report example of Bad ch, With more Jitter noise caused by FEXT

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Here is a table that summarizes the cross talk requirements for different generations of PCIe:

PCIe Generation	Adjacent Lane	Non-adjacent Lane
PCIe 5.0	-43 dB	-53 dB
PCIe 4.0	-40 dB	-50 dB
PCIe 3.0	-37 dB	-47 dB
PCIe 2.0	-34 dB	-44 dB
PCIe 1.0	-31 dB	-41 dB

Sheets로 내보내기

* Source https://bard.google.com/

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

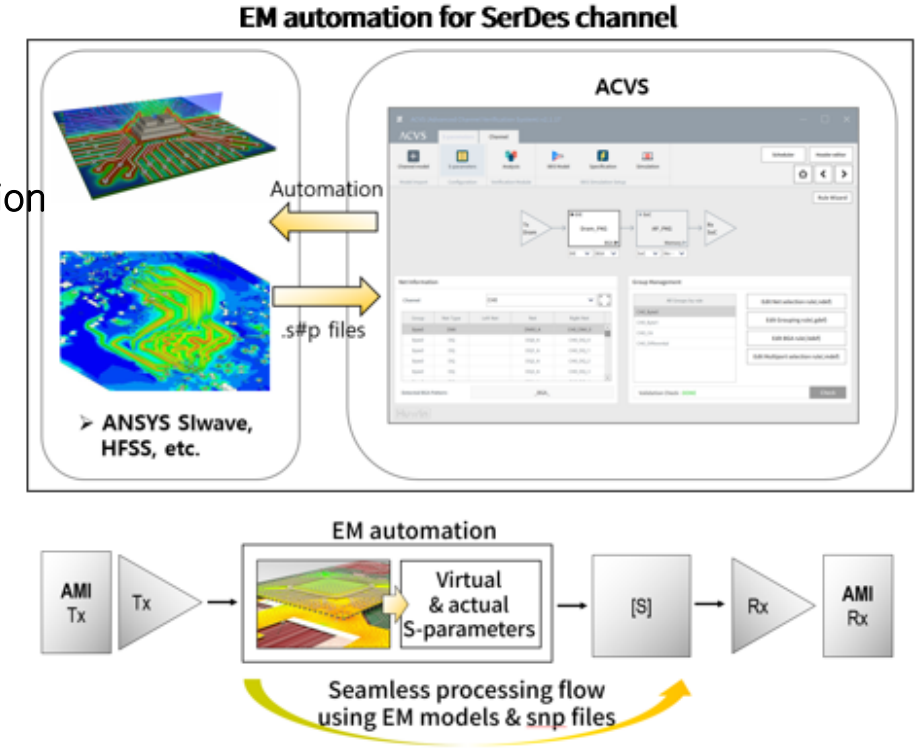
- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

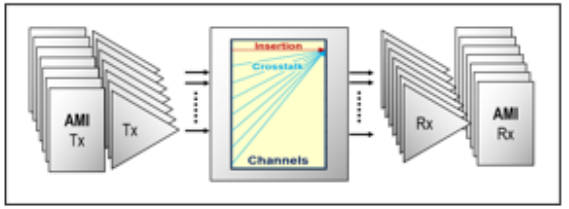
Huwin Update plan: Adv. SerDes Pack

Next wave for SI/PI

EM automation + Full X-talk SerDes AMI

- Fully integrated automation of ANSYS EM for SerDes channel
- **World 1st automation in SerDes AMI simulation including full X-talk**
- Applications: **PCIe Gen5, UFS**, etc.
- **EM automation: Released, General SerDes AMI: Released, Full X-talk SerDes AMI: 2023. 3Q**





The world 1st full X-talk automation in the SerDes AMI simulation. (2023.3Q)

5 to 6Gen High Speed Interconnection

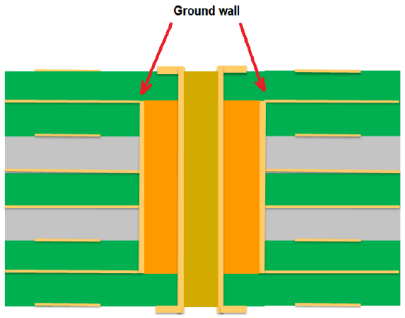
5 to 6Gen Tech. Issues :

Tech. Issues :

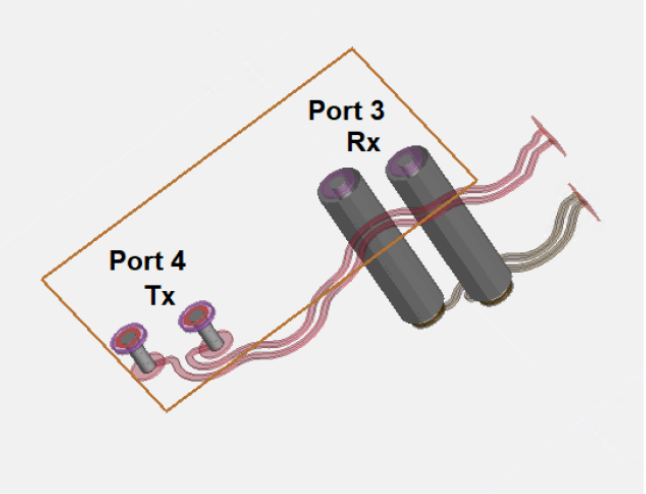
- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

PCIe 6.0 Platform Crosstalk Reduction :

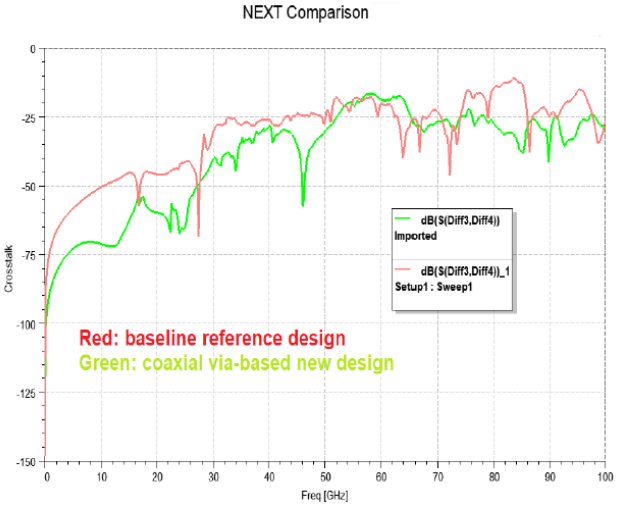
- Coaxial via protected PCIe 6.0 receive path



Coaxial via cross section view



Coaxial via protected PCIe 6.0 receive path



Near-end (NEXT) crosstalk comparison

* Source : SLIDES_Track07_DesignofaSIPIOptimizedPCIe _Final_Gao.pdf , DesignCon 2023

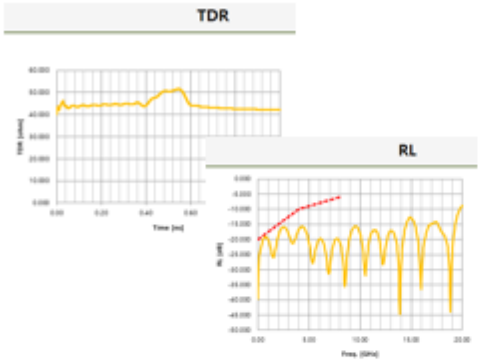
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

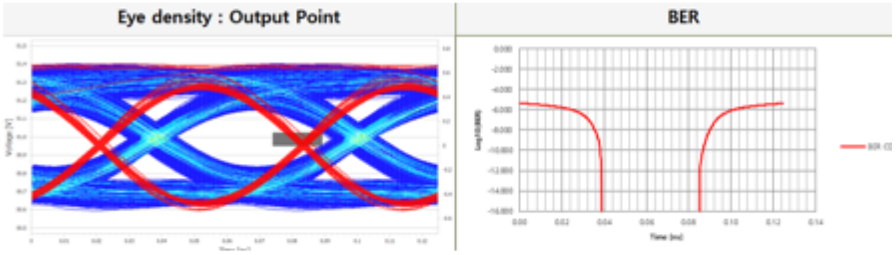
Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

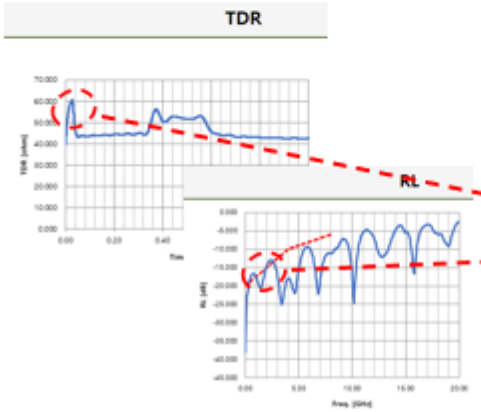
➢ **Huwin ACVS Basic SI (RL, TDT) and Eye/BER report results correlation example for Jitter analysis :**



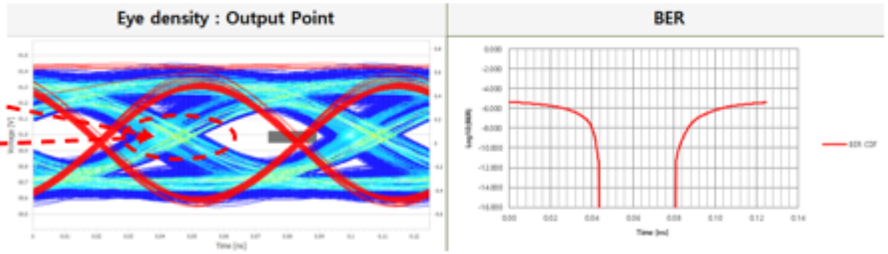
ACVS Basic report example of Good ch, Satisfy the TDR impedance/ RL limit (Return Loss)



ACVS EYE/BER report example of Good ch, With less Jitter noise



ACVS Basic report example of Bad ch, Over the TDR impedance/ RL limit (Return Loss)



ACVS EYE/BER report example of Bad ch, With more Jitter noise caused by Return Loss

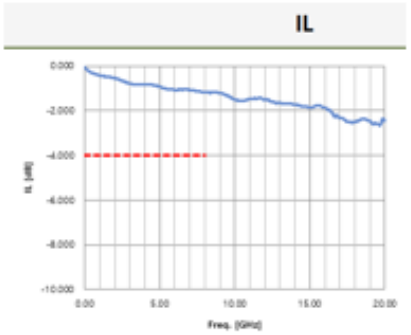
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

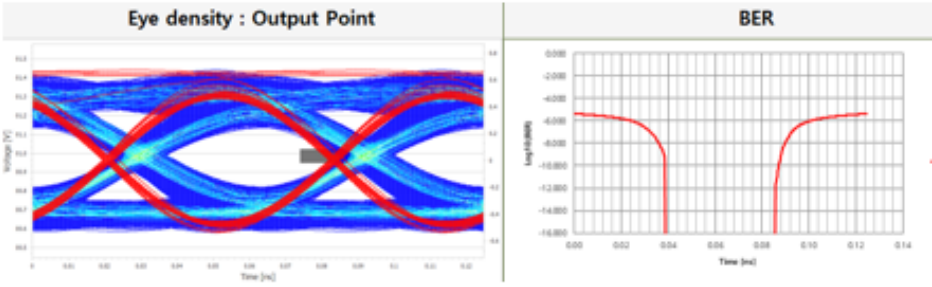
Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

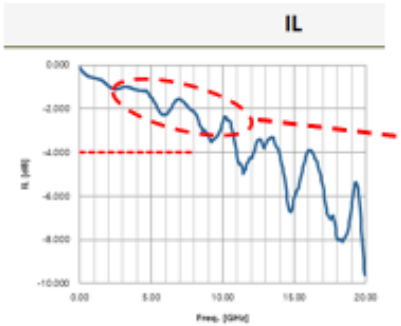
➢ **Huwin ACVS Basic SI (IL, ISI) and Eye/BER report results correlation example for Jitter analysis**



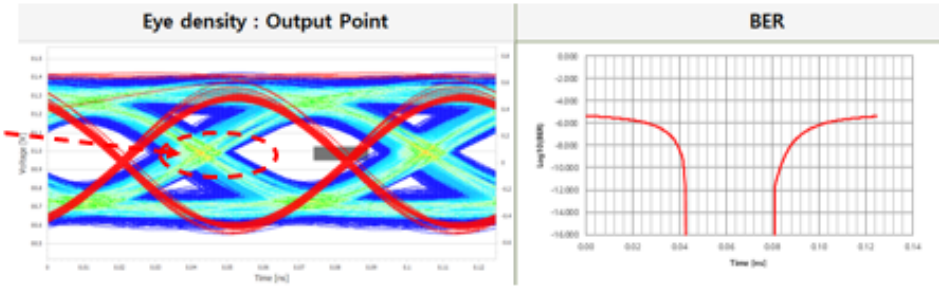
ACVS Basic report example of Good ch, Satisfy the IL limit (Insertion Loss)



ACVS EYE/BER report example of Good ch, With less Jitter noise



ACVS Basic report example of Bad ch, With more IL (Insertion Loss)



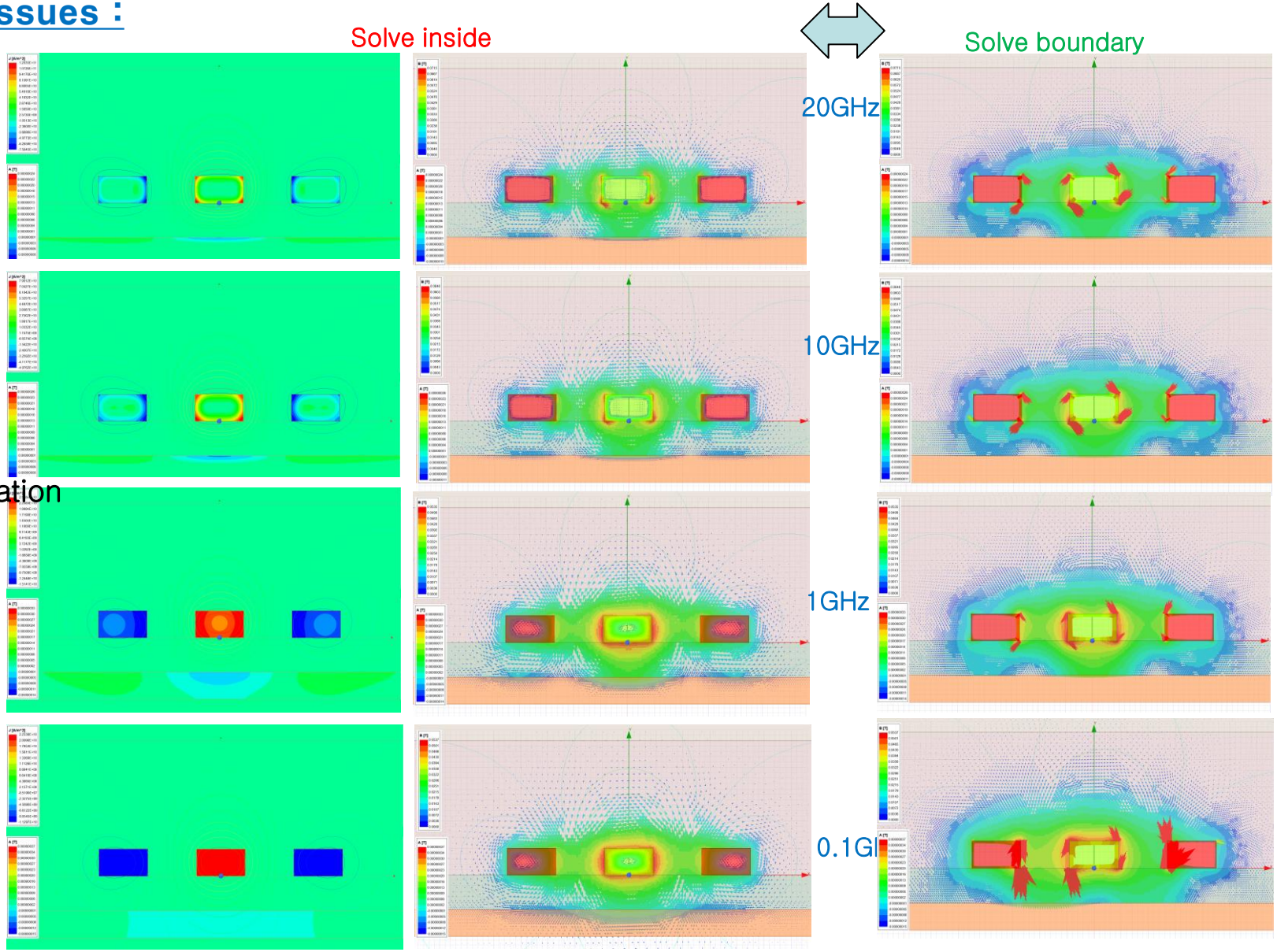
ACVS EYE/BER report example of Bad ch, With more Jitter noise caused by Insertion Loss or ISI

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification



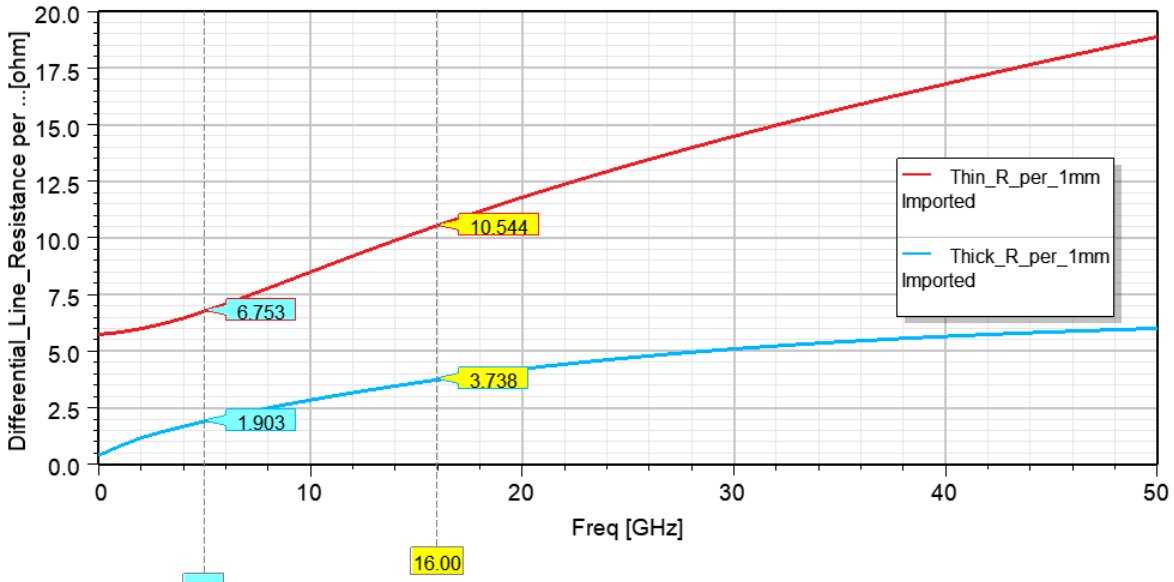
5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Fig. 6. Proposed RDL cross-section

* Source : Hybrid RDL Design in Fan-out Package, EPTC IEEE 2021, ASE



Thin, Thick RDL layer line resistance/mm vs. freq.

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

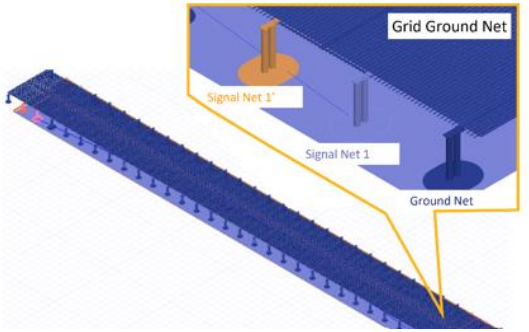
Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

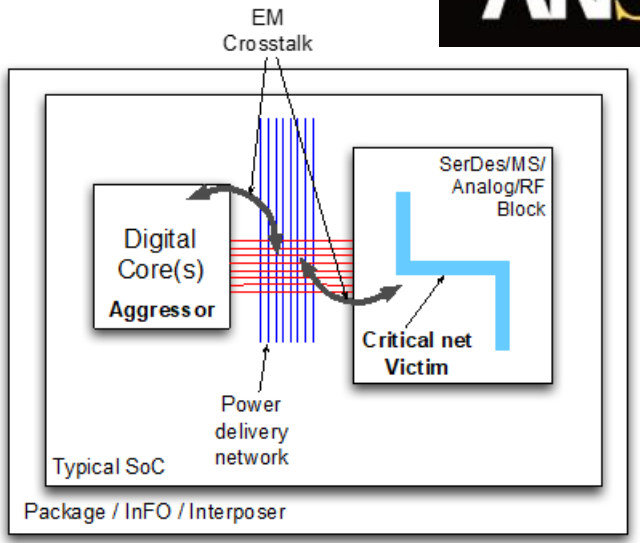
⇨ Helic Raptor-X integration to HFSS

HFSS

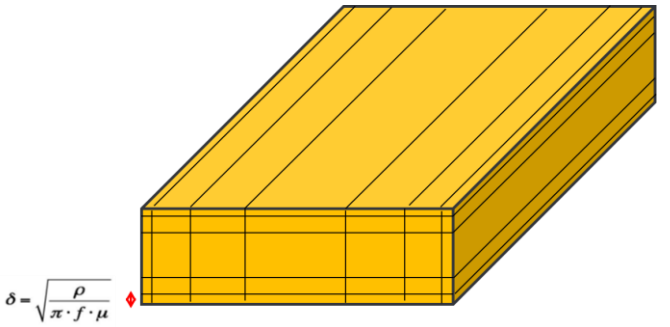
- HFSS 3D Layout integrations – Raptor-X, Q3D
  - Full IC design EM modeling & simulation w/Raptor-X
  - Q3D for package & PCB RLCG parasitic extraction
  - Model transfer to HFSS 3D Layout
    - Multiple EM solvers in 3D Layout (FEM, MoM/IE)
    - Full chip-to-system simulation



ANSYS Helic



* Source : ANSYS

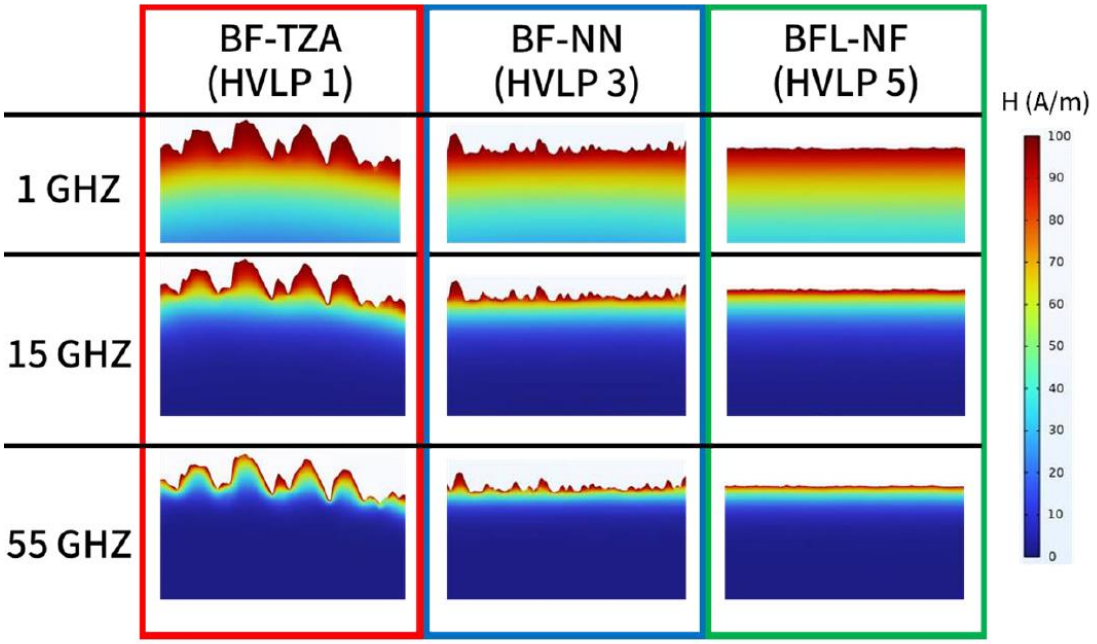


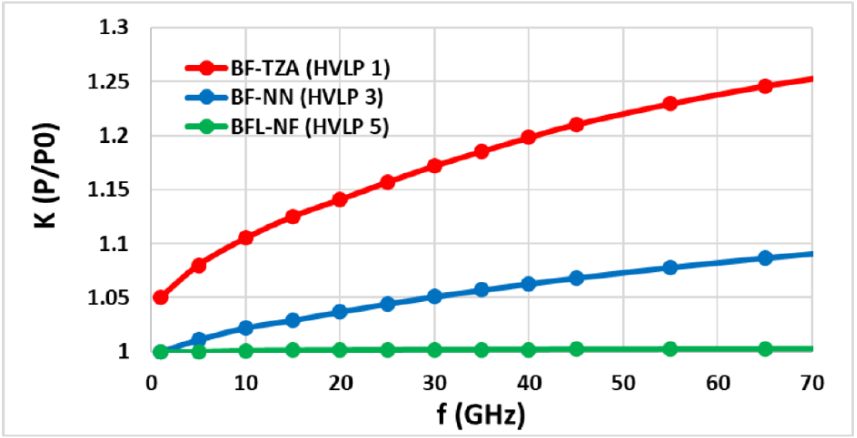
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification





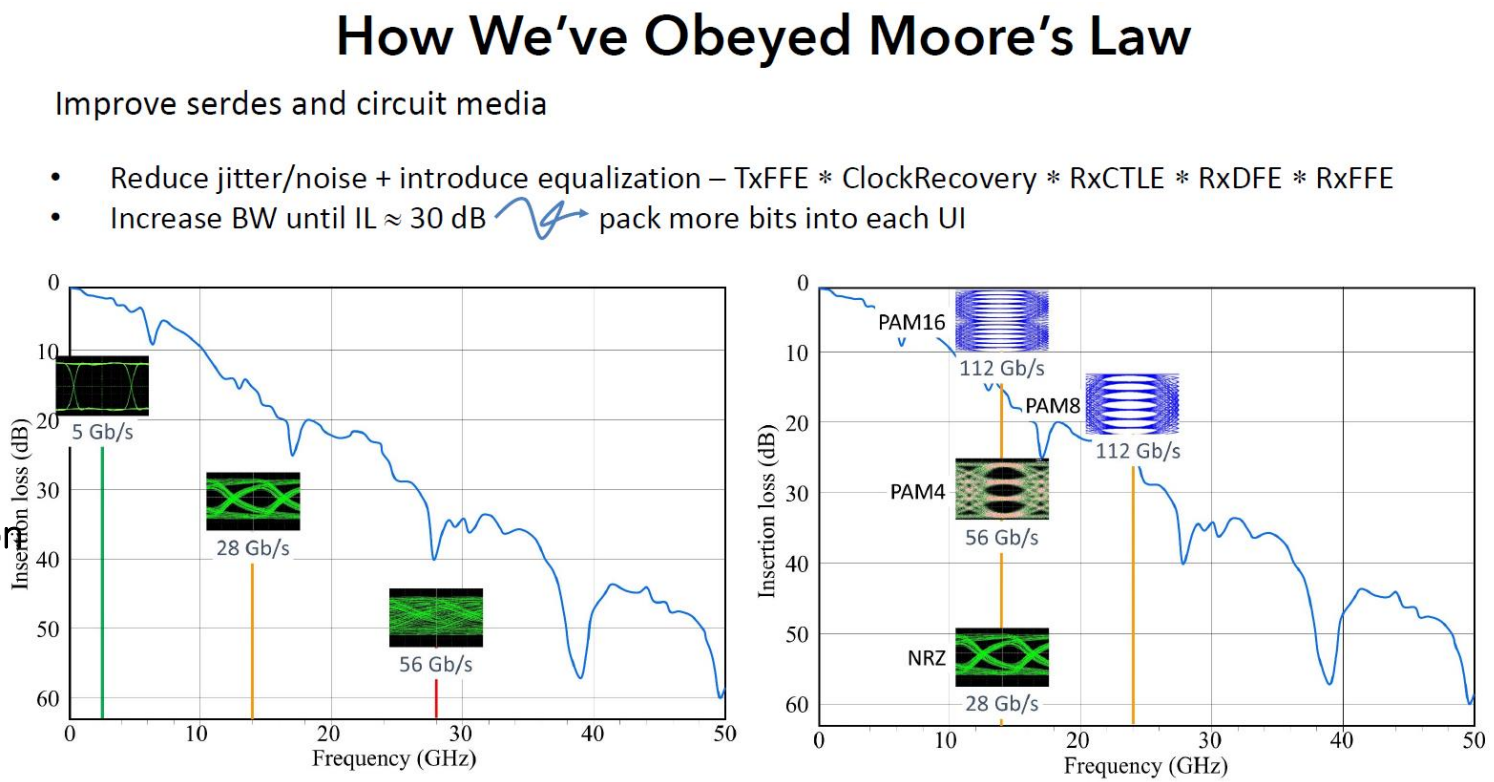
* Source : SLIDES_Track04_Finite element modelling of copper_Wittmann.pdf , DesignCon2023

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification



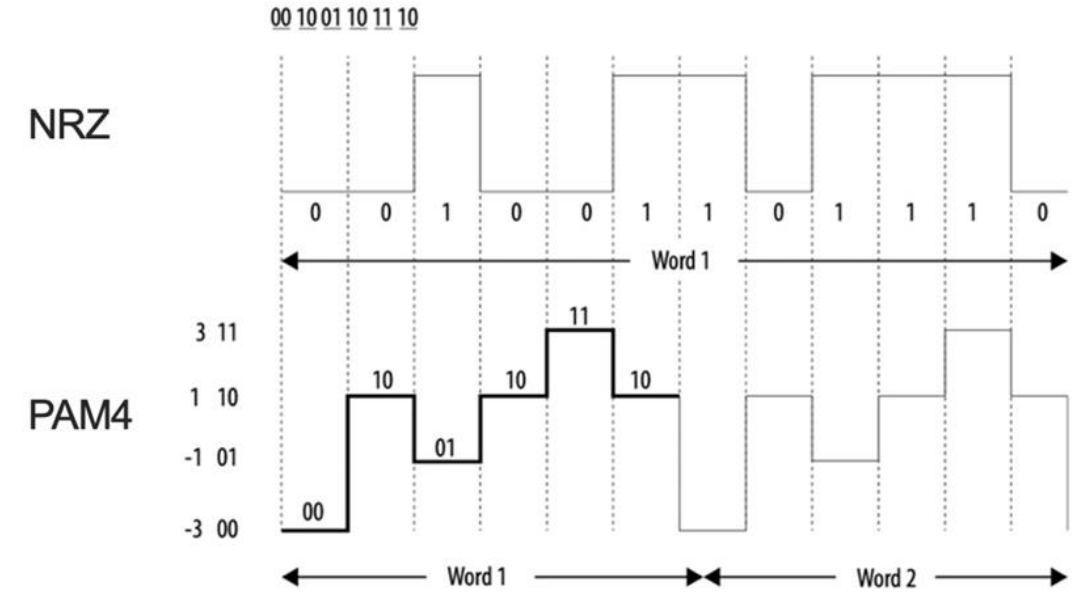
* Source : Designcon2022- Case of the Closing Eyes Panel 2022_FINAL.pdf

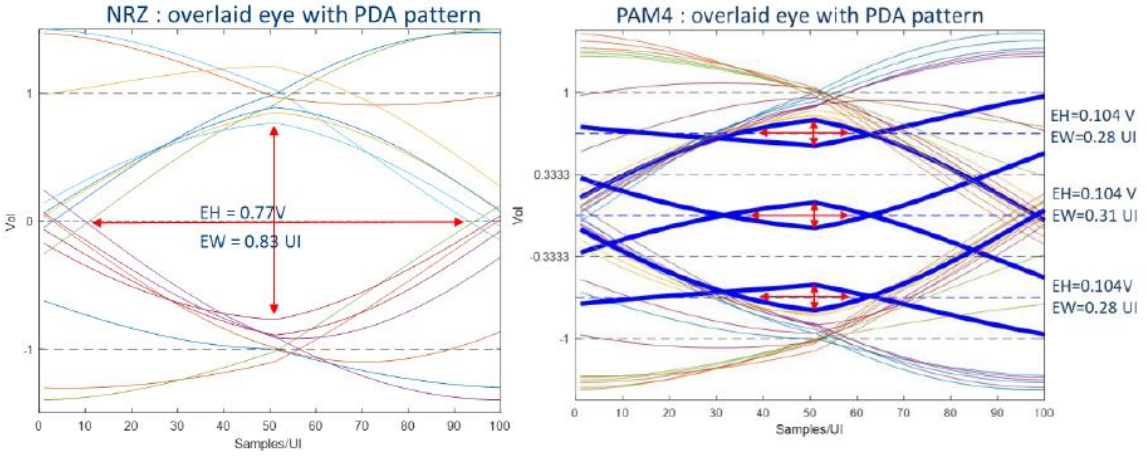
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification





* Source : Designcon2023- SLIDES_Track06_PCIe6.0(PAM4)SignalIntegrity_Liu.pdf

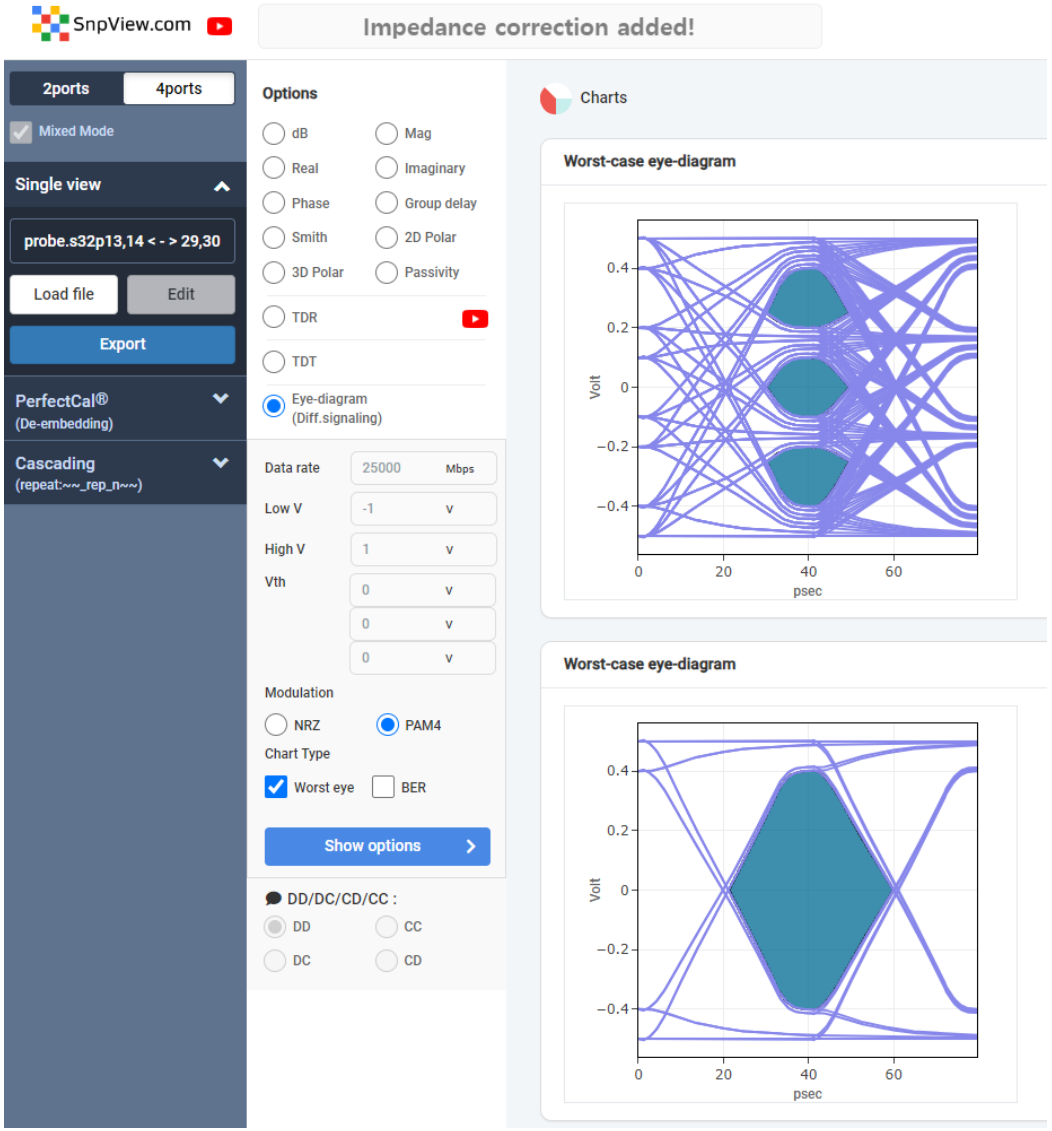
PAM4 signaling is more sensitive to cross-talk, signal reflections, and power supply noise

5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification



SnpView.com , PAM4 vs. NRZ Eye diagram

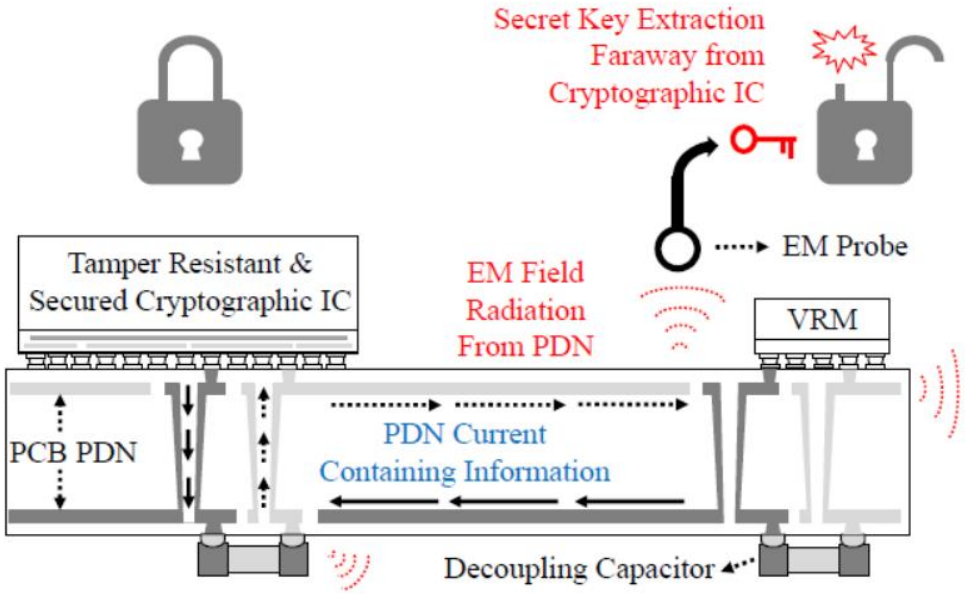
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Power Noise and EMI Issues in Hardware Security



- PDN is the path where power/ground currents flow to AES core, which resembles the operation behavior.
- As a result, radiation from the PCB PDN can cause EM information leakage issues.

* source : Electromagnetic (EM) & Interconnection Modeling and Analysis for SI/PI, EMC, Hardware Security, Prof. Youngwoo KIM, Sejong University

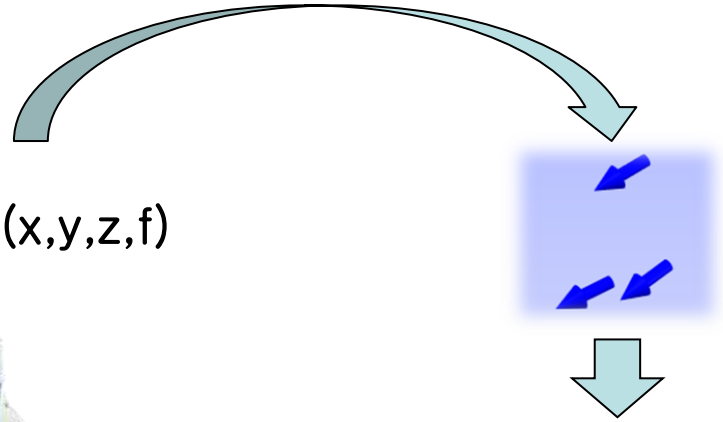
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

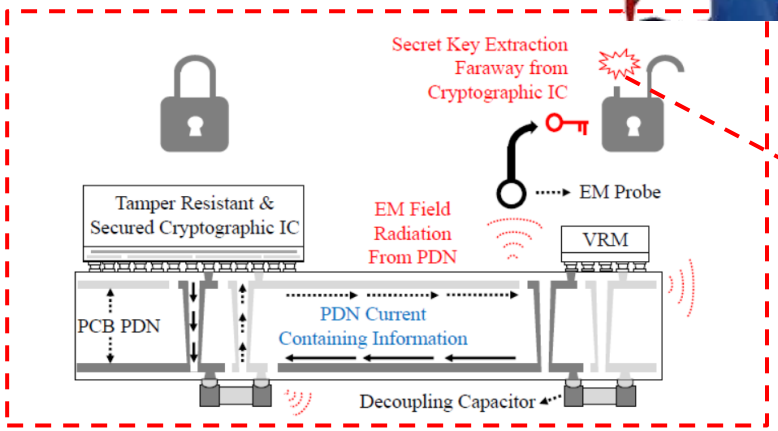
- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

EMCoS SRC3D toolkit :
Eq. magnetic dipole source (EM reconstruction)

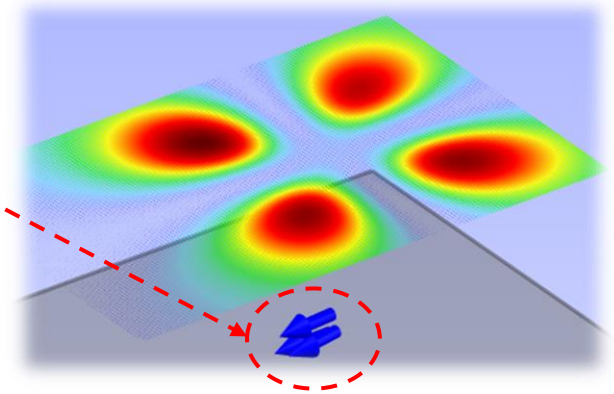


Hx_mag, Hy_mag (x,y,z,f)

Dipole source to 3D EM (HFSS)
=> Simulation/optimization to reduce the EMI



APREL EMI-Sight Scan @ Huwin



5 to 6Gen High Speed Interconnection

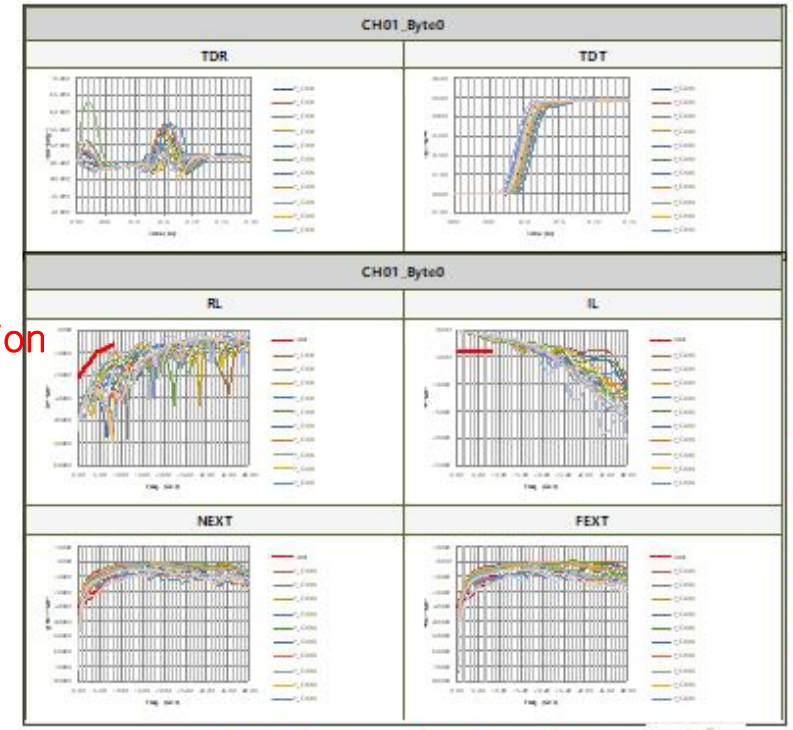
5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

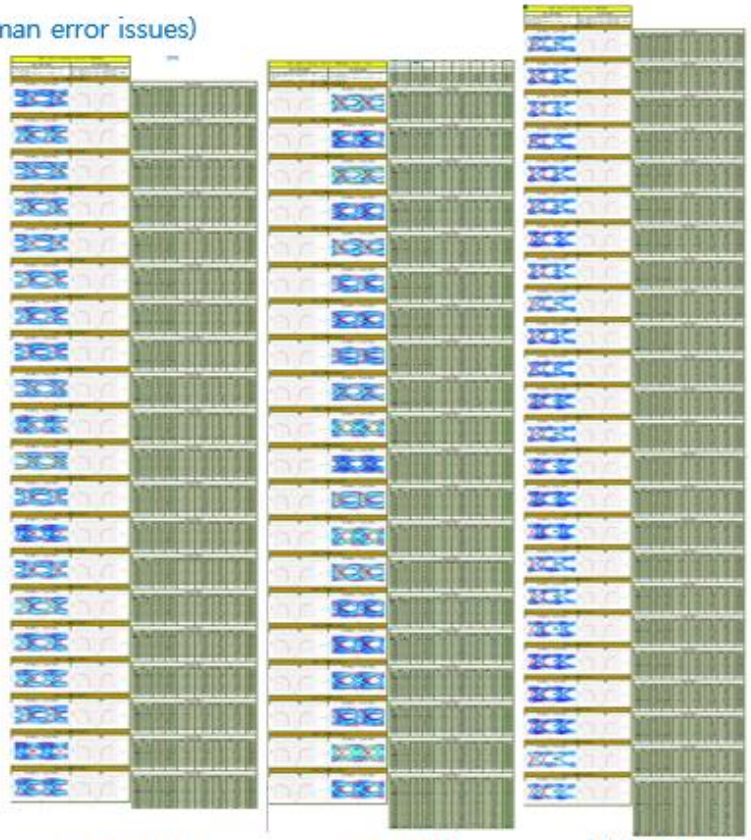
Huwin ACVS Case study-3: AI Chip Ch. Verification Issues (Single-ended AMI)

- AI Chip Complexity : PCIe Gen5(32Gbps x 32ch.), **GDDR6**(16Gbps, > 300 I/O nets), HBM3(6.4Gbps, 1024 I/O nets)
- Full Ch. X-talk sum, TDR, BER/Eye Verification needed
- Schematic base manual verification is difficult (time and human error issues)



Basic-SI: 2h. 40m (**GDDR6** Byte0~7)

ACVS Ch. Verification solution (GDDR6 total: ~10 hours)



Byte0 Write | Byte0 Read | Byte01 CA

AMI analysis: 6h.30m (**GDDR6** Byte0~7)

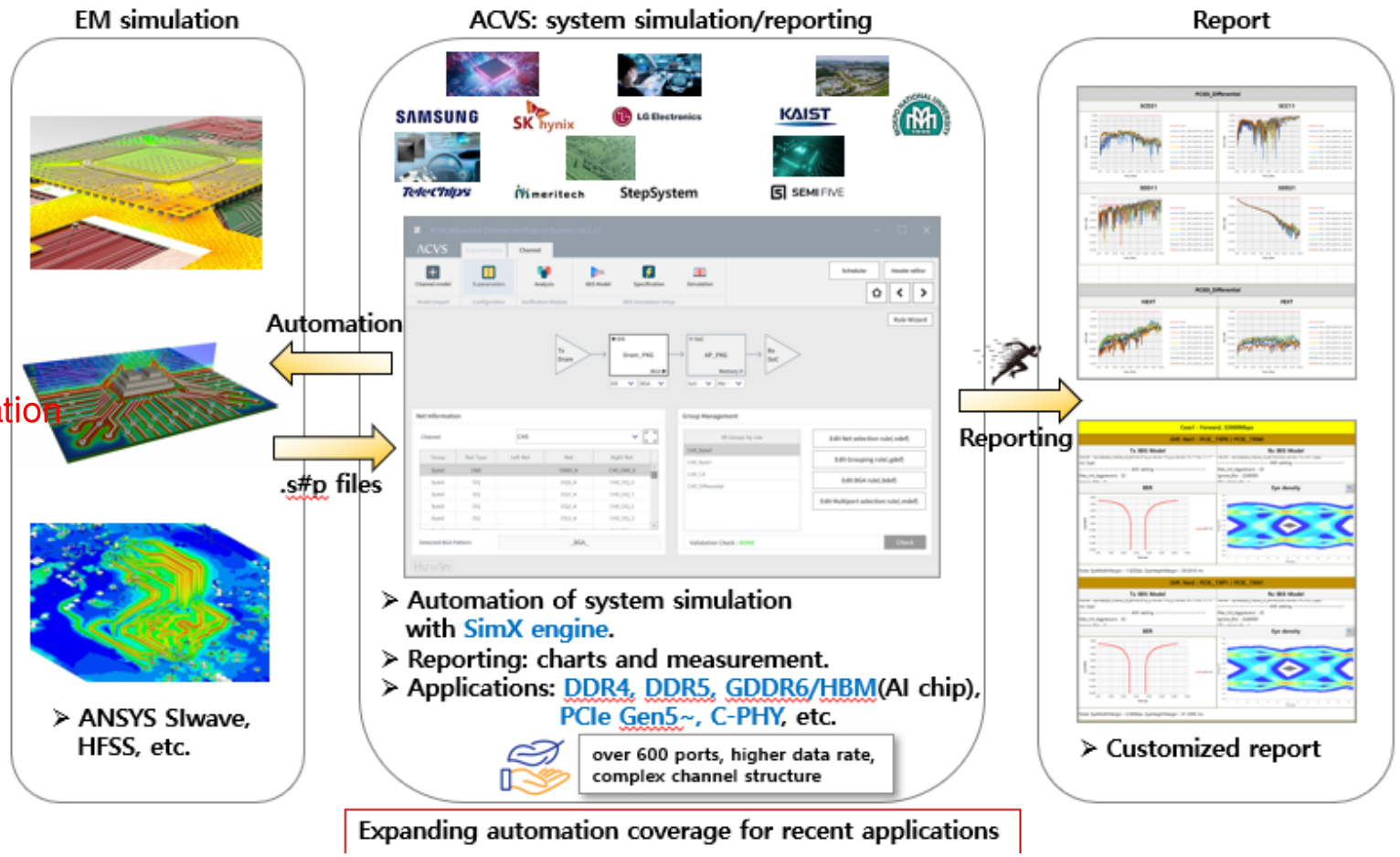
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

Huwin ACVS: The dedicated solution for SI/PI analysis with the high-speed channels

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification



5 to 6Gen High Speed Interconnection

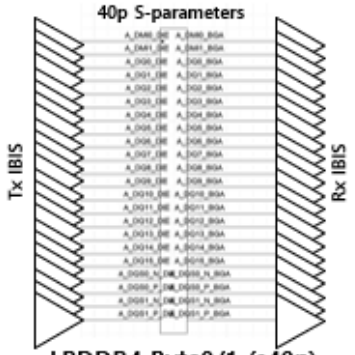
5 to 6Gen Tech. Issues :

Tech. Issues :

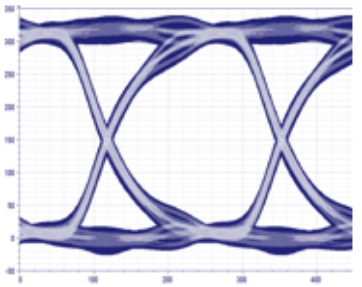
- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Huwin ACVS Case study-1: LPDDR4 (Transient)

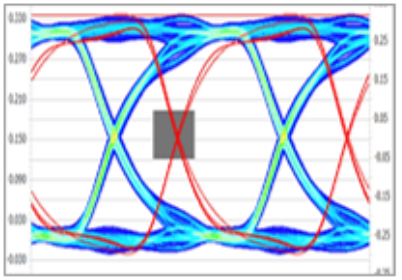
- 4.266Gbps, step->UI/32, sim. time-> **7.68us** (2^15 PRBS)
- Tx/Rx IBIS models: Non-linear model (Rising/falling waveform, pull-up/pull-down I/V data)
- Simulation environment: Intel i7 13700K, 32GB RAM



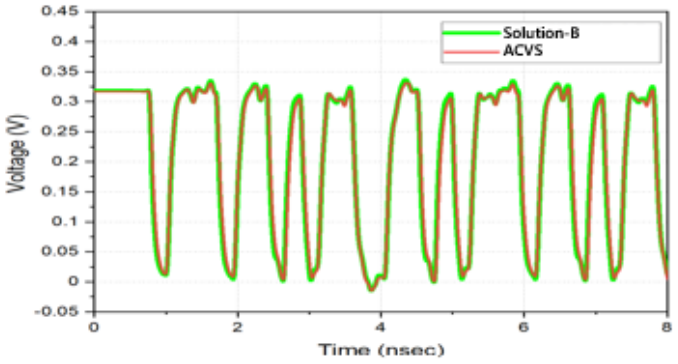
LPDDR4 Byte0/1 (s40p)
(Pkg+Board+Pkg)



Solution-B



ACVS



Solution type	Conditions	Analysis time
Solution-B	-manual setting (over ~30 min) -without reporting	27 hours
ACVS	-auto setting -auto reporting	**26 min**

x60 faster

Transient simulation comparison

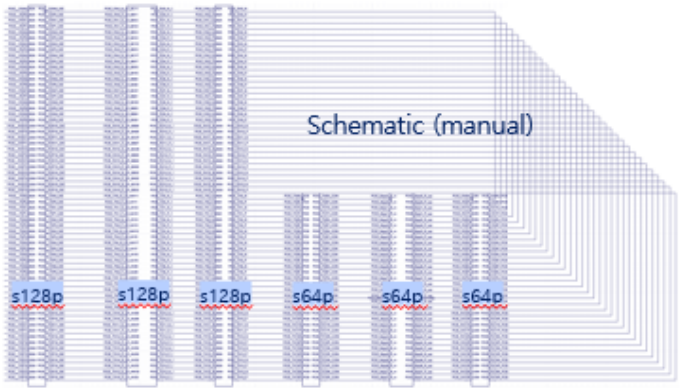
5 to 6Gen High Speed Interconnection

5 to 6Gen Tech. Issues :

Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

Huwin ACVS Case study-2: PCIe Gen5 channel (32 Gbps, IBIS-AMI)

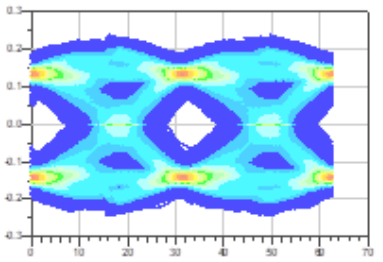


Tx/Rx AMI models + Channel S-parameters
PRBS: total 2,270,000 bits
(=ignore bits: 2,240,000+ input bits: 30,000)

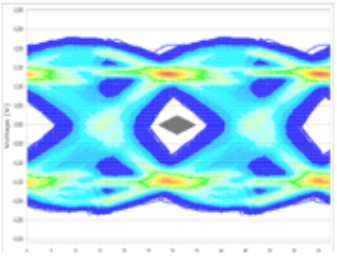
```
(Ignore_Bits (Usage Info) (Type Integer) (Default 2240000)
```

Solution type	Conditions	Analysis time
Solution-A	-manual setting (over ~1h) -without reporting	AMI: 9h 30m
ACVS	-auto setting -auto reporting	Basic-SI: 38m AMI: 3h 40m

Analysis results x2.6 faster



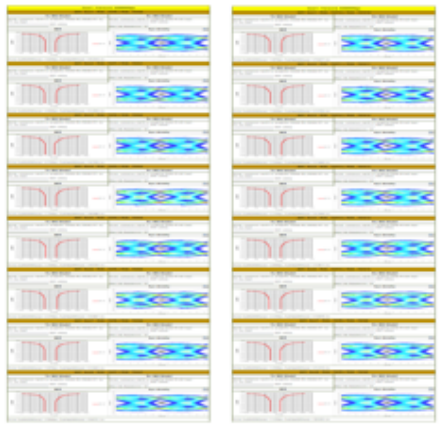
Solution-A



ACVS

Solution: ANSYS Ch. modeling + ACVS SI/PI analysis

Basic-SI: 38m



AMI: 3h 40m

Leading the Simulation Market for 50 Years

#1 IN ENGINEERING SIMULATION SOFTWARE

The Industry Leader

Simulation is Our Core Business

Uniquely Positioned for Growth

Setting the Gold Standard for Simulation Solutions

ANSYS Huwin

Thank You