Tech. Seminar :

시뮬레이션 통한 SI 설계 :
Advanced Silicon/Package/PCB Interconnection SI(Signal Integrity) Design

Huwin, 정성일
010-3381-1417, sijeung@huwin.co.kr

목차

1. Advanced Silicon/Package/PCB SI(Signal Integrity) 기술동향

2. 시뮬레이션 통한 SI 설계

3. DesignCon2024 자료 소개

2-1 : Crosstalk Noise Optimization For Robust 112G PAM4 Design in Stacked Silicon Interconnect Technology

2-2 : 224G Ultra-low Loss PCB Solution

2-3 : Enhancing End-to-End 224G Systems by Optimizing Metaconductors for Package Performance

2-4 : PCI Express & PAM4: The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems

2-5 : Mitigating crosstalk through the placement of Power-Ground Capacitors for DDR5 Memory

2-6 : EMI and Intentional-EMI Attacks against Power Delivery Network of Crypto/Information Devices

2-7 : Correlation methodology for 128 GT/s operation of PCIe ® 7.0 DSP-based IBIS-AMI models

2-8 : m-TL Circuit Model of 5/6G Connectors for Fast Resonance Crosstalk Analysis

2-9 : Using Fast Multipole Methods to Speed Up S-Parameter Transient Simulation

2-10 : E-Tube : RF Plastic Dielectric Waveguide for Terabit High-Speed Interconnect

2-11 : Survey on Correlation & Simulation Methodologies for PCB Structures Through 67GHz

2-12 : A Novel PCB Footprint for Double-Sides press-fit Stacked Optical Module Application

2-13 : DDR5 System CA Margin Risk and Mitigation

2-14 : Vertical Conductive Structure (VeCS) Technology: Simulation and Measurement

1. Advanced Silicon/Package/PCB SI 기술동향

5 to 6Gen 동향 :

Cloud computing, AI, 5G, IoT

HBM, TSV

Advanced Silicon/Package/PCB/Connector/Cable

1Gbps-NRZ to 224 Gbps-PAM4

Modulation vs. Channel vs. FEC

Return path -> Cross-talk

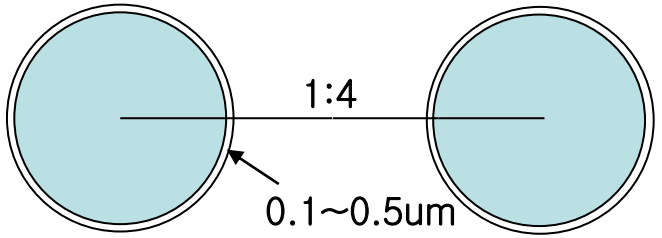
Design Optimization -> Characterization

Trise : BW/5 => Z0 matching 이 필요해지는 거리

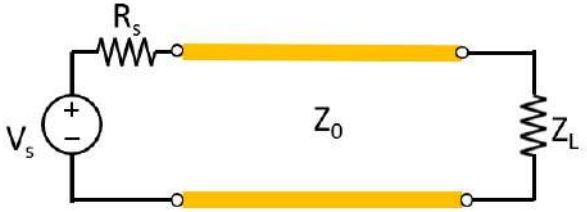
10Gbps -> 20ps => 0.5mm
32Gbps -> 6ps => 0.15mm
56Gbps -> 4ps => 0.1mm

<10um 지름, 50um 높이

TSV to TSV : 1:2.5 to 1:4 (diameter to pitch)



Technology Scale 에 따른 R(f),L(f),C(f),G(f) ?



$$V(z) = V_0^+ e^{-\gamma z} \qquad \frac{dV(z)}{dz} = -(R + jwL)I(z)$$

$$I(z) = I_0^+ e^{-\gamma z} \qquad \frac{dI(z)}{dz} = -(G + jwC)V(z)$$

$$\frac{dV(z)}{dz} = -(R + jwL)I(z) = -(R + jwL)\, I_0^+ e^{-\gamma z} = -\gamma V_0^+ e^{-\gamma z}$$

$$Z_0 = \frac{V_0^+}{I_0^+} = \frac{-(R+jwL)}{-\gamma} = \frac{(R+jwL)}{\sqrt{(R+jwL)(G+jwC)}} = \sqrt{\frac{(R+jwL)}{(G+jwC)}}$$

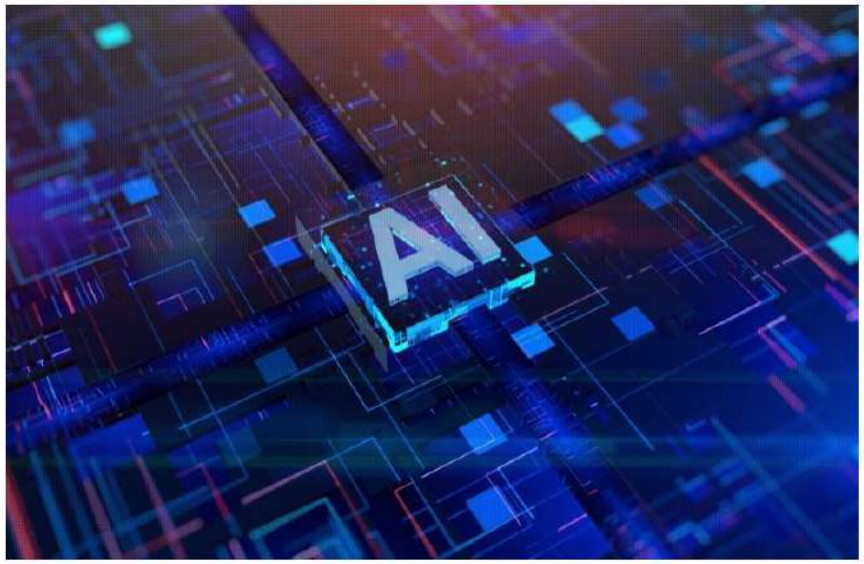
1. Advanced Silicon/Package/PCB SI 기술동향

5 to 6Gen 동향 : Chiplet AI

네패스, 칩렛 이종 집적 초고성능 AI 반도체 개발 과제 '낙점'

서재창 기자 sjed@hellot.net | 등록 2023.05.16 15:28:18 URL복사

[무료교육 마감임박] AI융합 제조산업 현장 빅데이터 디지털전환 전문인력 양성과정 (7월 진행)



사피온, 포항공대, 광주과학기술원(GIST) 등과 컨소시엄 구성해 개발 추진

네패스가 추진한 '칩렛 이종 집적 초고성능 AI 반도체 개발' 과제가 과학기술정통부 주관 국가공모에 선정됐다.

네패스가 총괄 및 1세부를 맡은 이번 사업은 AI 반도체 설계업체인 사피온, 포항공대, 광주과학기술원(GIST) 등과 컨소시엄을 구성해 개발을 추진하게 된다. 사피온이 AI용 NPU(Neural Processing Unit)를 개발하고, 다수의 소자를 네패스가 칩렛 패키지로 구현하는 프로젝트다.

* Source : https://www.hellot.net/news/article.html?no=78002

Huwin ACVS :

Advanced (AI) Chip Verification System

HBM3
UCIe
PCIe Gen6
EM (ANSYS) 해석 자동화
Eye-diagram 최적화 위한 Tx/Rx 모델

1. Advanced Silicon/Package/PCB SI 기술동향

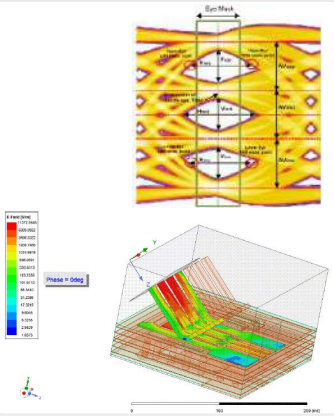
5 to 6Gen 동향 : 6G 네트워킹

Huwin :

100/200Gbps 급 신호 무결성 백플레인 기술
(레인당 200G/400G/800G 지원)

[국내/세계최초] 112G급/224G급 백플레인 설계 기술 개발[공동연구2(휴윈)+주관]

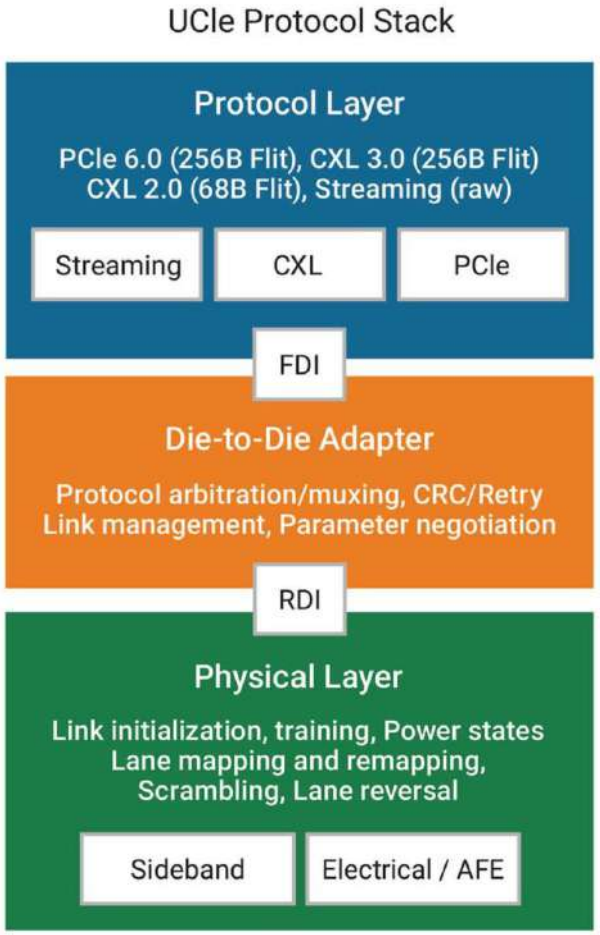
- 224Gbps 속도를 가능하게 하는 Cable 및 백플레인 커넥터(Paladin HD 224)등이 2023년도부터 개발되어 현재 샘플이 가용하며, 224Gbps 속도를 가능하게 하는 PCB 재질이 개발 중인 기술적 환경에서 112Gbps는 국내최초 설계를 추진하며, 세계최초 224Gbps급 SerDes 설계에 도전(주관+공동연구2)
- 이를 가능하게 하기 위하여 설계와 검증을 위한 Full cross-talk 특성이 반영된 Multi SerDes 초광대역 채널 통합 분석 SW를 자체개발하여 적용하는 세계최초의 사례(공동연구2)

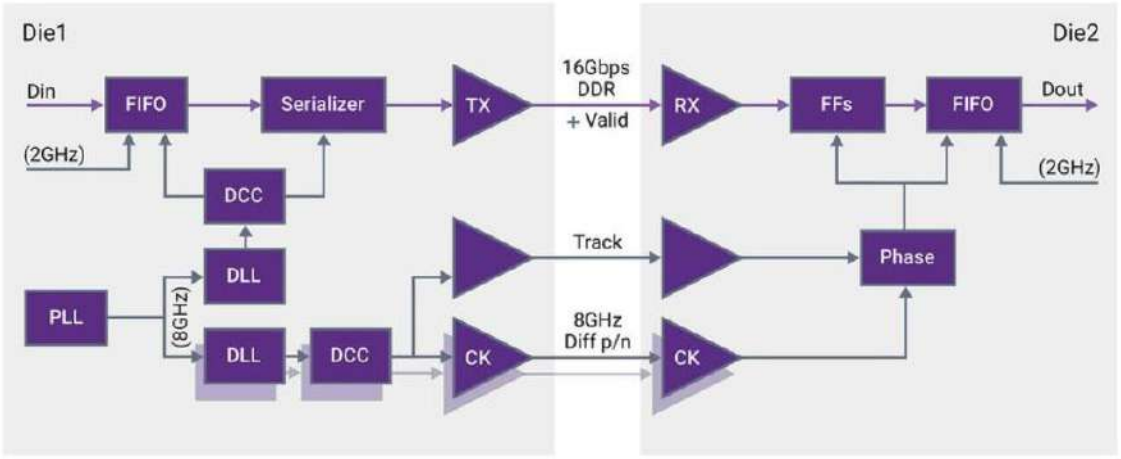


1. Advanced Silicon/Package/PCB SI 기술동향

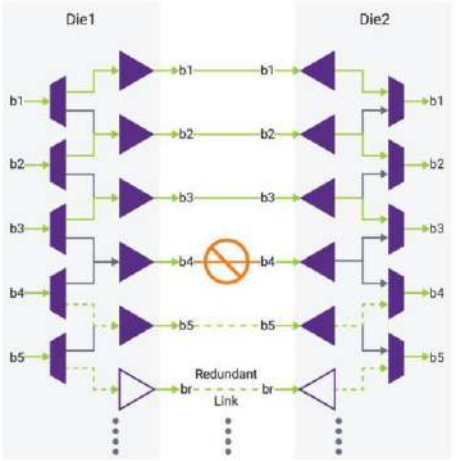
UCIe : Standard Package ⇨ Advanced Package

UCIe for advanced packages (silicon interposer, silicon bridge or RDL fanout)
UCIe for standard packages (organic substrate or laminate)





Clock pair를 제외하고 모두 single-endded



Adv. Pkg에는 Redundant pin이 존재하고
일반 pin fail시에 Rerouting 역할

Fig. 5: The Physical Layer tests each die connection to determine failure and re-routes signals to a redundant pin.

1. Advanced Silicon/Package/PCB SI 기술동향

UCIe :

Advanced Package

Standard Package

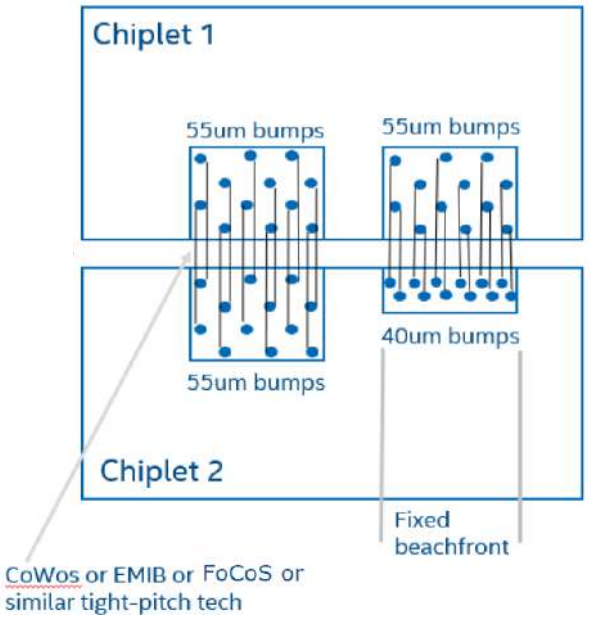
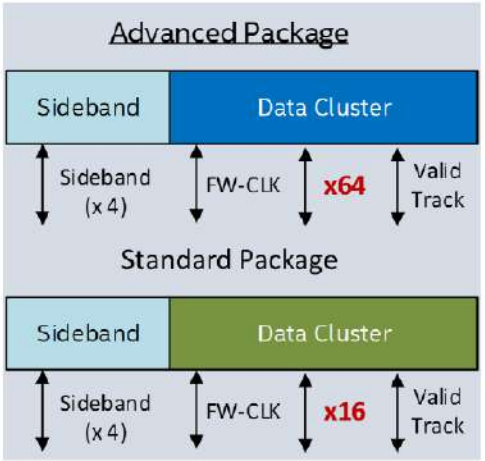


Table 1: UCIe 1.0 Characteristics and Key Metrics

Characteristics / KPIs	Standard Package	Advanced Package	Comments
Characteristics			
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	
Target for Key Metrics			
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u for AP; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm²)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ CXi Flit Mode

Adapter+PHY 전체 delay



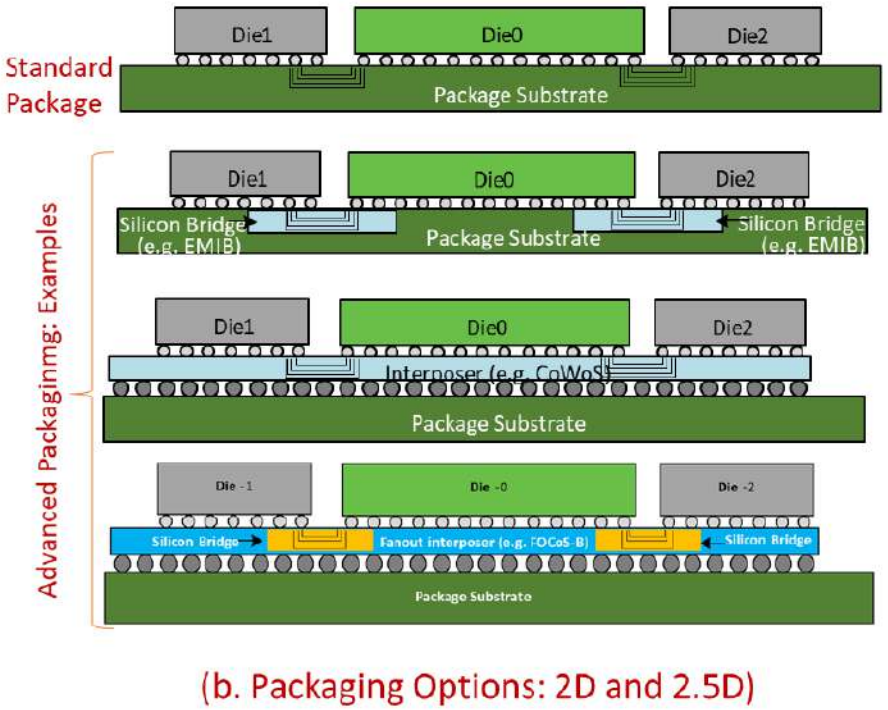
Die - 1		Die - 2			
x16	<-->	x16	CL-0 x16	<-->	CL-0 x16
x32	<-->	x32	CL-0 x16	<-->	CL-0 x16
			CL-1 x16	<-->	CL-1 x16
x64	<-->	x64	CL-0 x16	<-->	CL-0 x16
			CL-1 x16	<-->	CL-1 x16
			CL-2 x16	<-->	CL-2 x16
			CL-3 x16	<-->	CL-3 x16

(1, 2, or 4 Clusters can be combined in one UCIe Link)

Figure 6: Cluster Width; 1, 2, or 4 Clusters can be combined in each packaging option to deliver higher bandwidth

1. Advanced Silicon/Package/PCB SI 기술동향

UCIe : Standard Package ⇨ Advanced Package



(b. Packaging Options: 2D and 2.5D)

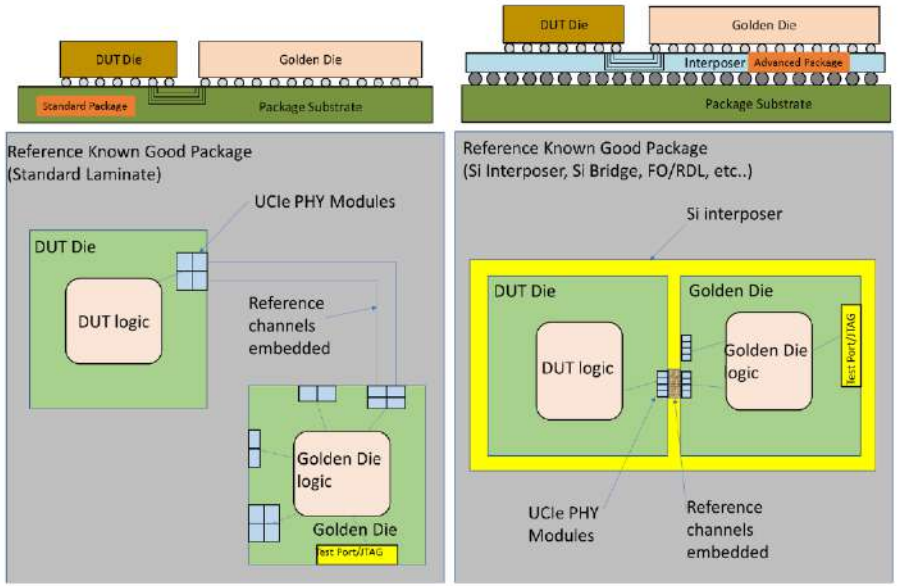


Figure 4: UCIe Compliance – both standard and advanced packaging

The unit of construction of the interconnect is a cluster which comprises of N single-ended, unidirectional, full-duplex Data Lanes (N = 16 for standard package and 64 for advanced package), one single-ended Lane for Valid, one lane for tracking, a differential forwarded clock per direction, and 2 lanes per direction for sideband (single-ended, one 800 MHz clock and one data). The advanced package supports spare lanes to handle faulty lanes (including clock, valid, sideband, etc) where as the standard package supports width degradation to handle failures.

PCIe PHY have a power efficiency of ~10pJ/b today which can be lowered by up to 20X with the UCIe based designs due to their shorter channel reach.

Sideband-> 1 data, 1 clock (SDR operation)
모두 Single-ended

1. Advanced Silicon/Package/PCB SI 기술동향

UCIe : Standard Package ⇨ Advanced Package

Figure 5-1. x64 and x32 Advanced Package Module

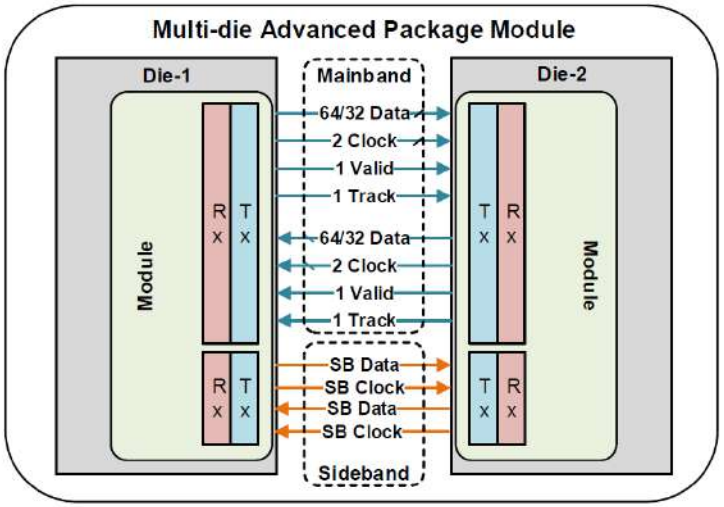
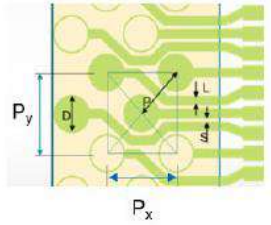


Figure 5-2. Standard Package Module

두 type모두 clock을 제외하고 모두 single-ended pin

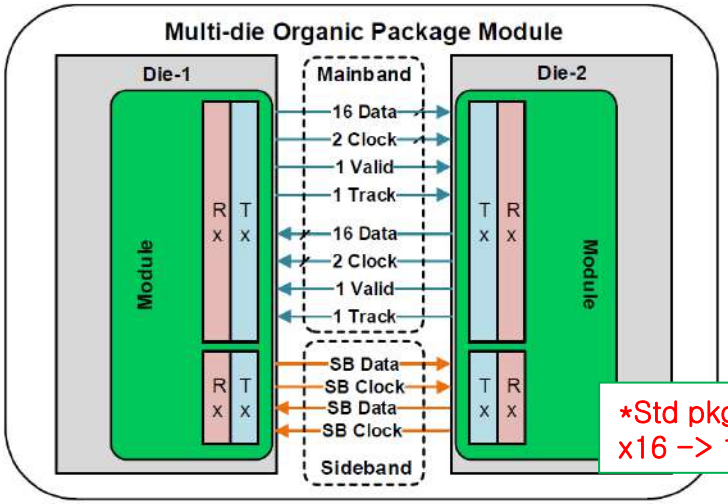
*Adv pkg
x64 -> 64 data + 4 redundant pin
x32 -> 32 data + 2 redundant pin



$P = D + L + 2S$
$P_y = D + 3L + 4S$

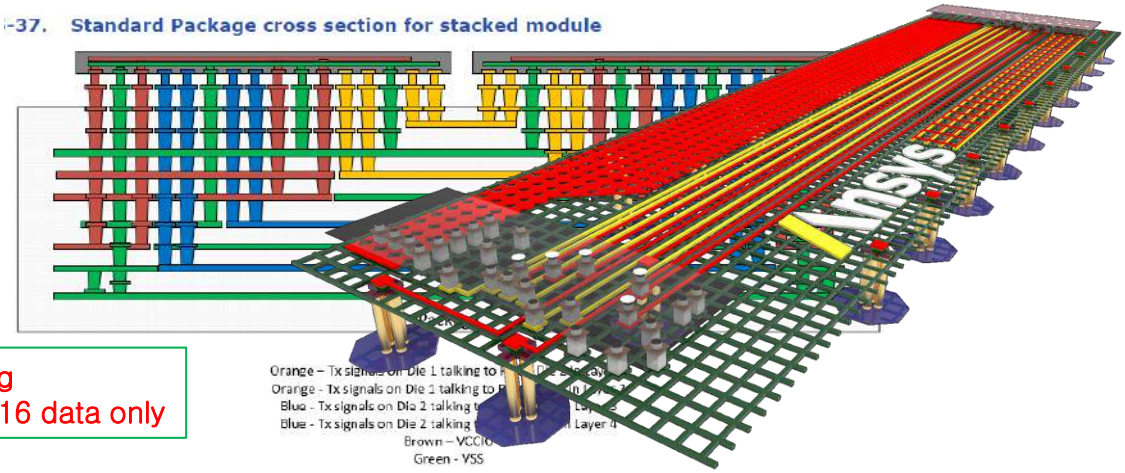
-36. Standard Package x32 interface: Signal exit routing

Layer 1	Tx	0	1	2	3	trk	vld	12	13	14	15	15	14	13	12	vld	trk	3	2	1	0	Rx
Layer 2	Module 1	4	5	6	7	ckp	ckn	8	9	10	11	11	10	9	8	ckn	ckp	7	6	5	4	Module 1
Layer 3	Rx	0	1	2	3	trk	vld	12	13	14	15	15	14	13	12	vld	trk	3	2	1	0	Tx
Layer 4	Module 2	4	5	6	7	ckp	ckn	8	9	10	11	11	10	9	8	ckn	ckp	7	6	5	4	Module 2
Sideband		m1txdatasb				m2rxdatasb		m1txcksb		m2rxcksb		m2txcksb		m1rxcksb		m2txdatasb			m1rxdatasb			Sideband



*Std pkg
x16 -> 16 data only

-37. Standard Package cross section for stacked module



1. Advanced Silicon/Package/PCB SI 기술동향

UCIe : Advanced Package

IMPLEMENTATION NOTE

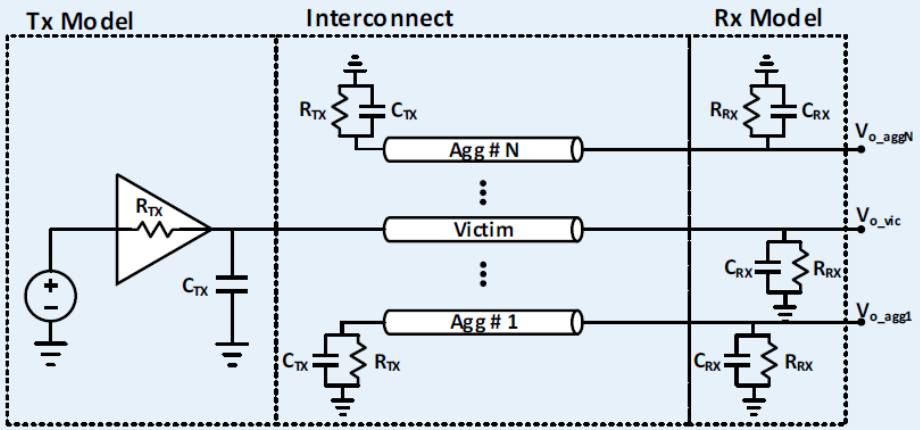
Figure 5-15 shows an example circuit setup that can be used to generate the statistical eye diagram shown in Figure 5-14. RTX is the Transmitter impedance and RRX represents the Receiver termination. CTX, CRX represent effective Transmitter and Receiver capacitance, respectively. For crosstalk, the 19-largest aggressors need to be included. Transmitter equalization (TXEQ) is enabled at 24 GT/s and 32 GT/s.

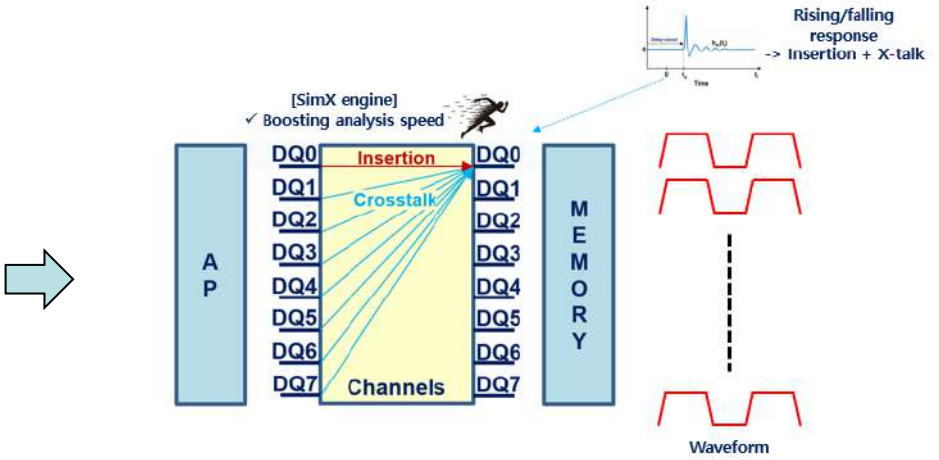
The eye diagram was generated using a two-step process.

1. Generate ISI and XTALK channel step response using circuit setup shown in Figure 5-15.
2. Use the generated channel response in a signal-integrity or channel-simulation tool to generate a statistical eye diagram (see Figure 5-14)

Other equivalent methods may be used, depending on the signal-integrity or channel-simulation tool.

Figure 5-15. Example Eye Simulation Setup





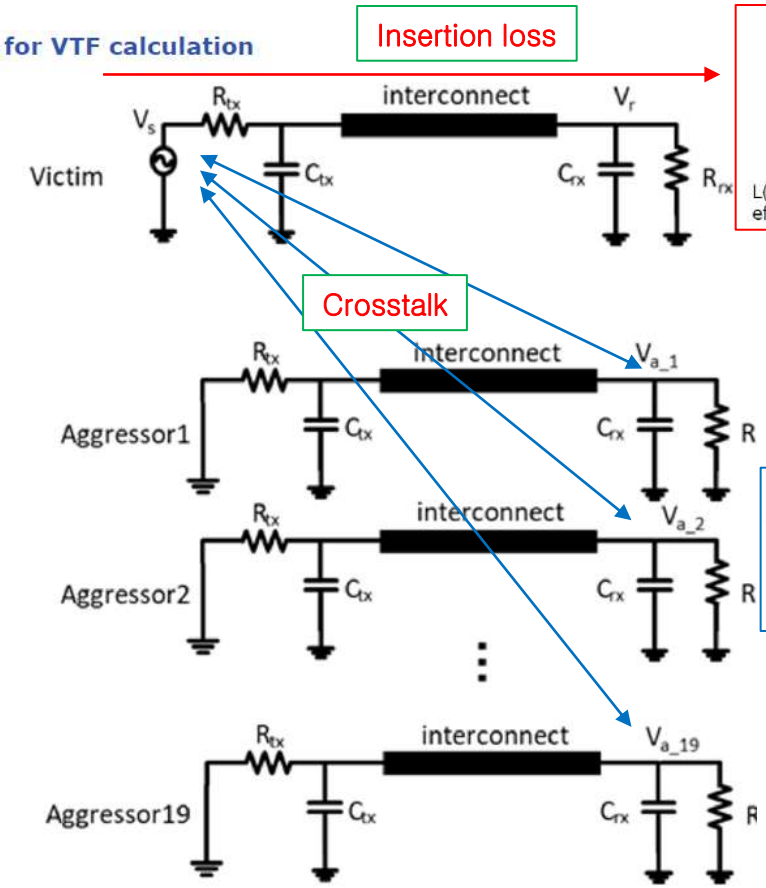
*Eye-diagram 분석 가이드
1. 왼쪽 회로구성으로 직접 Step response를 추출
2. 상용 시뮬레이터 이용

1. Advanced Silicon/Package/PCB SI 기술동향

UCIe : Standard Package ⇨ Advanced Package

Voltage Transfer Function (VTF) based metrics are used to define insertion loss and crosstalk. VTF metrics incorporate both resistive and capacitive components of TX and RX terminations.

Figure 5-16. Circuit for VTF calculation



$$L(f) = 20\log 10\left|\frac{V_r(f)}{V_s(f)}\right|$$

$$L(0) = 20\log 10\left(\frac{R_{rx}}{R_{tx}+R_{channel}+R_{rx}}\right)$$

L(f) is the frequency dependent loss and L(0) is the DC loss. For unterminated channel, L(0) is effectively 0.

VTF crosstalk is defined as the power sum of the ratios of the aggressor Receiver voltage to the source voltage. 19 aggressors are included in the calculation. Based on crosstalk reciprocity, VTF crosstalk can be expressed as:

$$XT(f) = 10\log 10\left(\sum_{i=1}^{19}\left|\frac{V_{ai}(f)}{V_s(f)}\right|^2\right)$$

Reciprocity이용하여 Vai/Vs 로 계산함
(Vai/Vs = Vs/Vai)

UCIe : Standard Package ⇨ Advanced Package

5.7.2 Advanced Package

Table 5-10. Channel Characteristics

Data Rate	4-16 GT/s	24, 32 GT/s
VTF Loss (dB)	$L(f_N) > -3$	$L(f_N) > -5$
VTF Crosstalk (dB)[1]	$XT(f_N) < 1.5\ L(f_N) - 21.5$ and $XT(f_N) < -23$	$XT(f_N) < 1.5\ L(f_N) - 19$ and $XT(f_N) < -24$

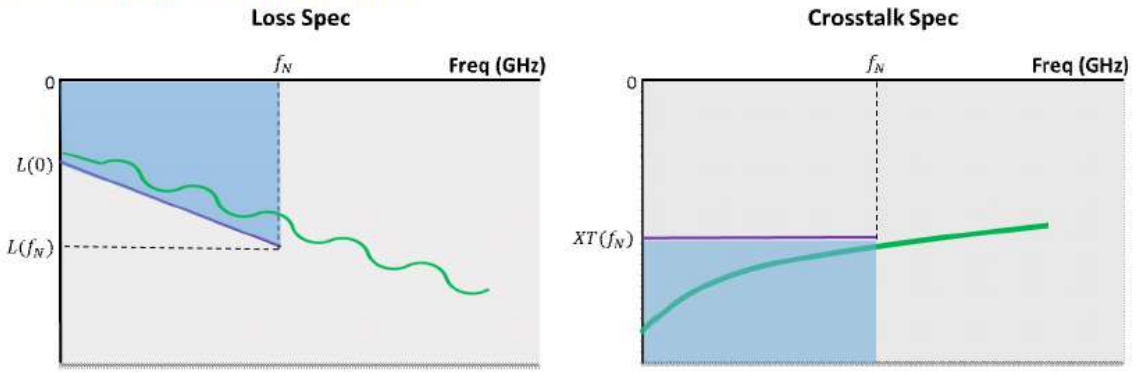
1. Based on Voltage Transfer Function Method (Tx: 25 ohm / 0.25 pF; Rx: 0.2 pF).

f_N is the Nyquist frequency. The equations in the table form a segmented line in 2-D map of loss and crosstalk, defining the pass/fail region.

f_N = fundamental freq. (ex. 4Gbps –> f_N =2GHz)

Figure 5-17. Loss and Crosstalk Mask

Insertion loss @ DC 계산 값

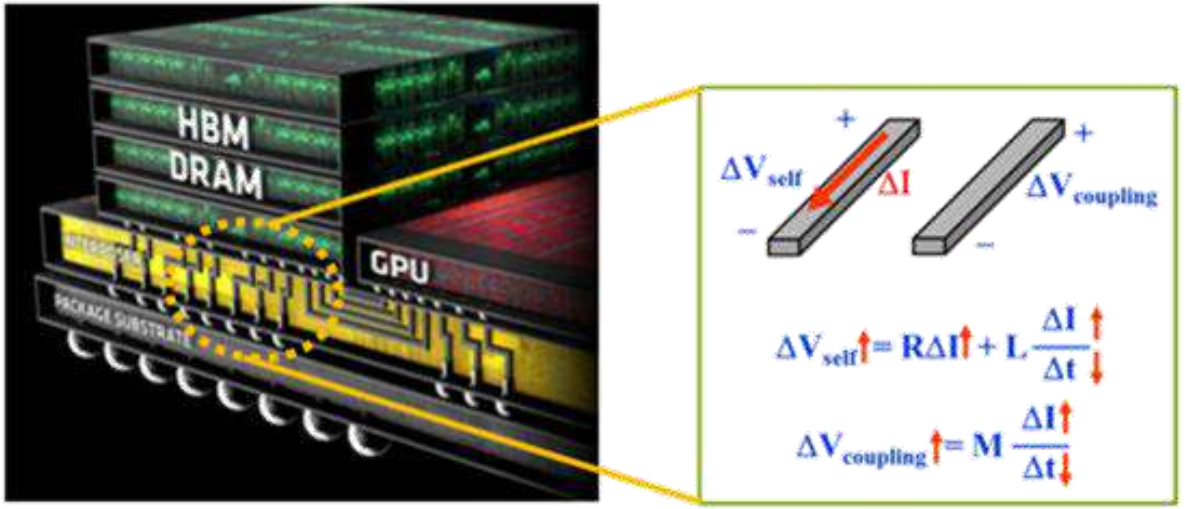


1. Advanced Silicon/Package/PCB SI 기술동향

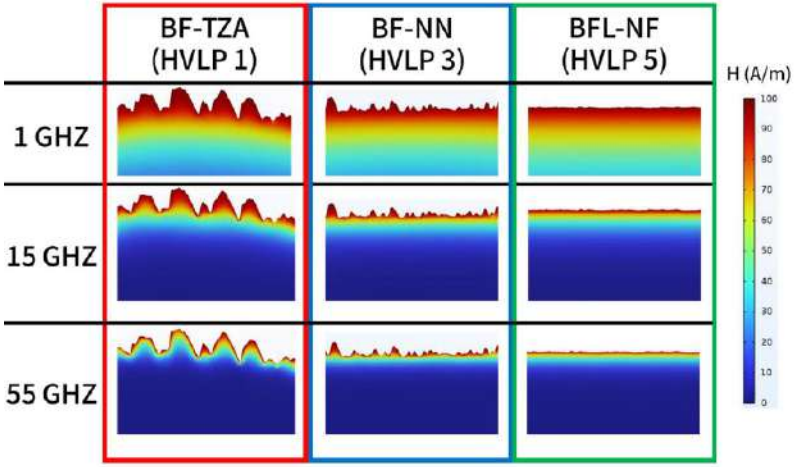
5 to 6Gen Tech. Issues : Advanced Package

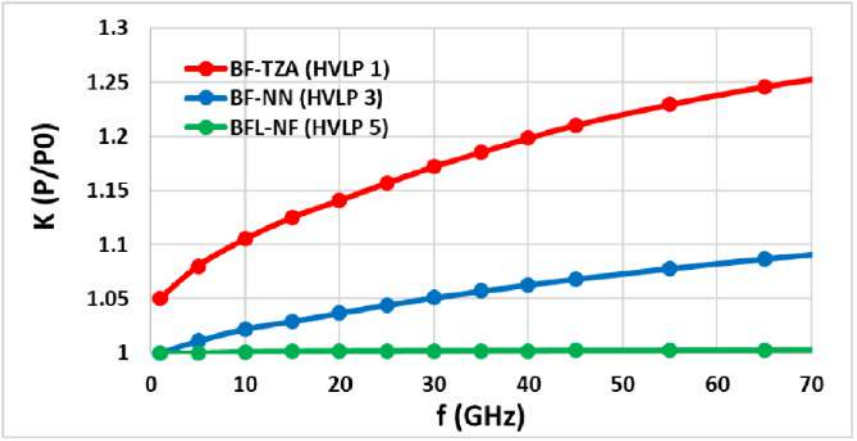
Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- Return path
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification



- **Smaller size & Narrower space**





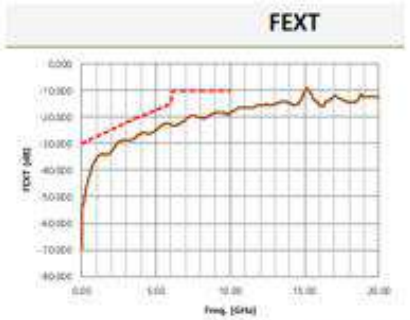
* Source : SLIDES_Track04_Finite element modelling of copper_Wittmann.pdf , DesignCon2023

5 to 6Gen Tech. Issues : Advanced Package

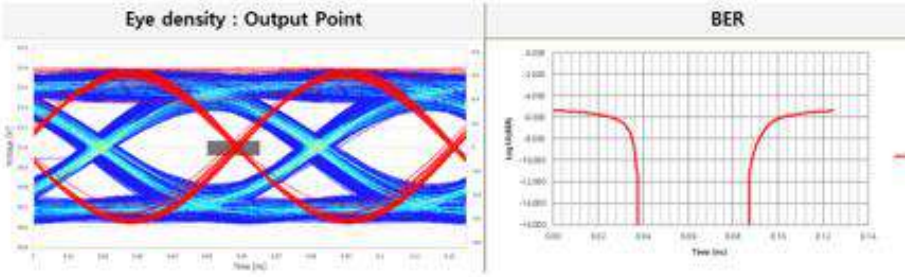
Tech. Issues :

- S-parameters
- Impulse Response
- Jitter
- X-talks
- Return path
- RL,TDT
- IL
- Skin Effects
- PAM4
- Hardware Security
- Full Ch. Auto verification

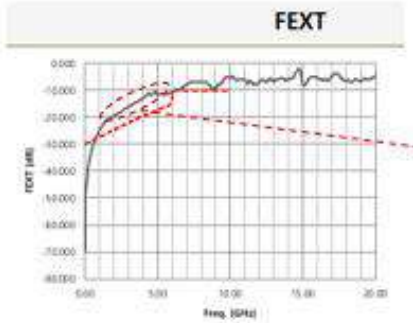
➢ Huwin ACVS Basic SI (FEXT) and Eye/BER report results correlation example for Jitter analysis



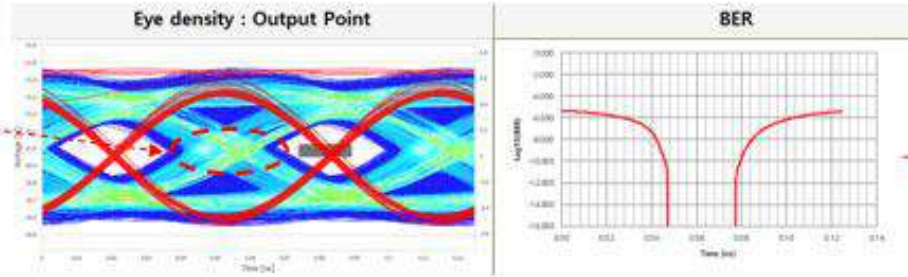
ACVS Basic report example of Good ch, Satisfy the FEXT limit (far end cross-talk summation)



ACVS EYE/BER report example of Good ch, With less Jitter noise



ACVS Basic report example of Bad ch, Over the FEXT limit (far end cross-talk summation)



ACVS EYE/BER report example of Bad ch, With more Jitter noise caused by FEXT

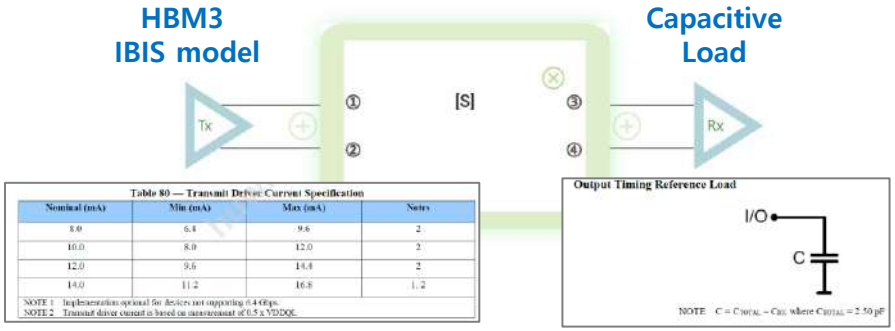
1. Advanced Silicon/Package/PCB SI 기술동향

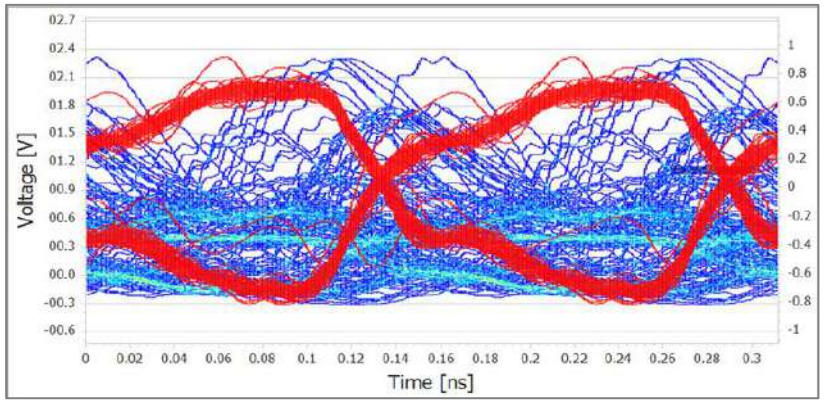
HBM3 : Advanced Package

. Advanced Package 분석을 위한 Eye-diagram/BER 분석 모듈 개발

: ACVS Transient solver (SimNX) 개선

-> HBM3 IBIS model 발산 억제 및 연산 효율성 개선 기술 개발

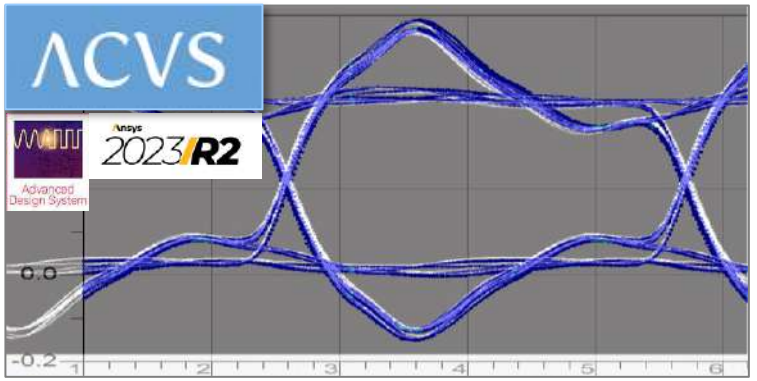




HBM3 Driver strength 14 mA 사례

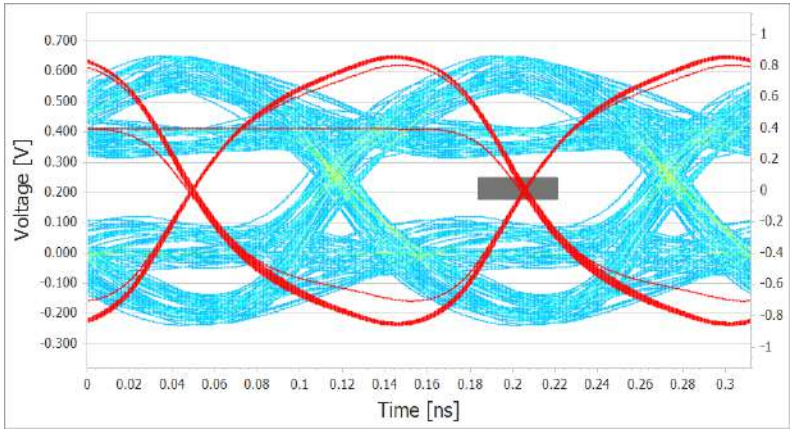
-> Solver 발산 이슈 발생

-> 발산 및 연산 속도 저하 문제



개선된 ACVS Transient solver (SimNX) 결과 검증

➢ 발산 문제 해결

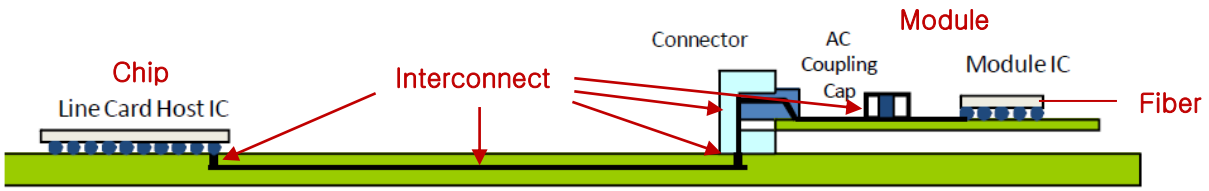


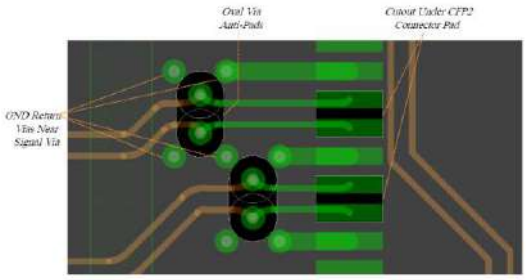
HBM3 test 분석 사례 (ACVS)

➢ Tx 14 mA, Rx capacitive load 조건 (6.4 Gbps), 발산 이슈 해결

1. Advanced Silicon/Package/PCB SI 기술동향

CEI-112G





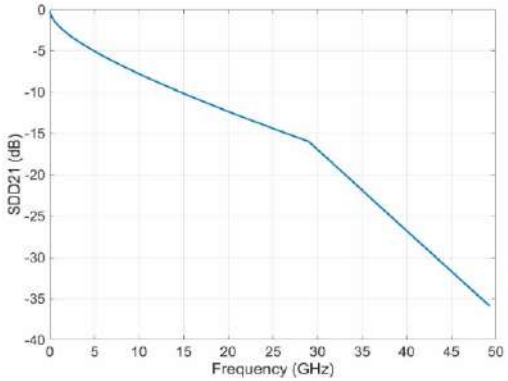
PCB design guide

112Gbps PAM4 Chip to Module interface :

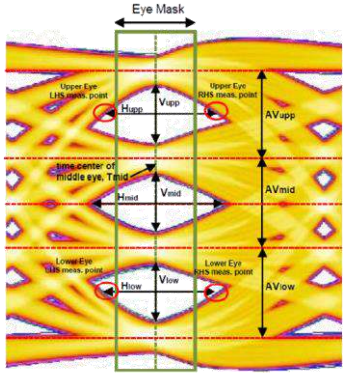
SI 최적화 대상 -> PCB trace, Vias, AC coupling Capacitor, Connector, copper Cable

=> Electrical spec. : Ch. Loss, Impedance, Eye Height/Width

=> 3D EM 분석을 통해 Electrical Spec. 을 만족하도록 최적화 설계 및 검증이 필수임
=> Cost effective 설계 구현을 위해 적절한 재질 선정 및 interconnection 설계가 매우 중요함



Ch. Loss (SDD21 of end-to-end limit) :
* ~80GHz 3D EM 분석 통한 Loss, Impedance 최적화 설계 필요함.

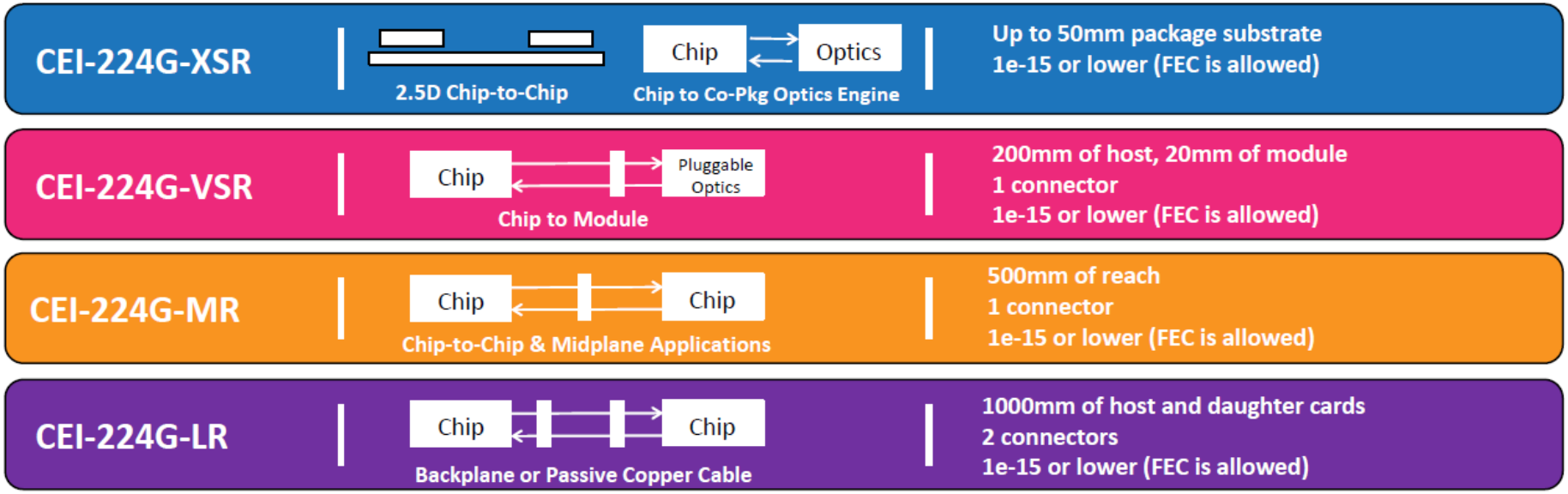


PAM4 signal Eye Parameters :
* PAM4의 경우 NRZ 대비 noise margin 이 30%이상 감소하므로, cross-talk, reflections, power noise 를 최소화 하도록 설계하여야 함.

1. Advanced Silicon/Package/PCB SI 기술동향

CEI-224G

- SerDes IO 대역폭은 2018년 100~112Gbps 에 이르고, 백플레인 길이는 40인치까지 도달됨.
- CEI-224G : 2020년 OIF Q3 미팅에서 차세대 224Gbps 급 프로젝트 승인 => 2022년 Q1 OIF 에서 신규 프로젝트 시작함. (CEI-224G-LR : Backplane or Passive Copper Cable, 1000mm of host and daughter cards 2 connectors)



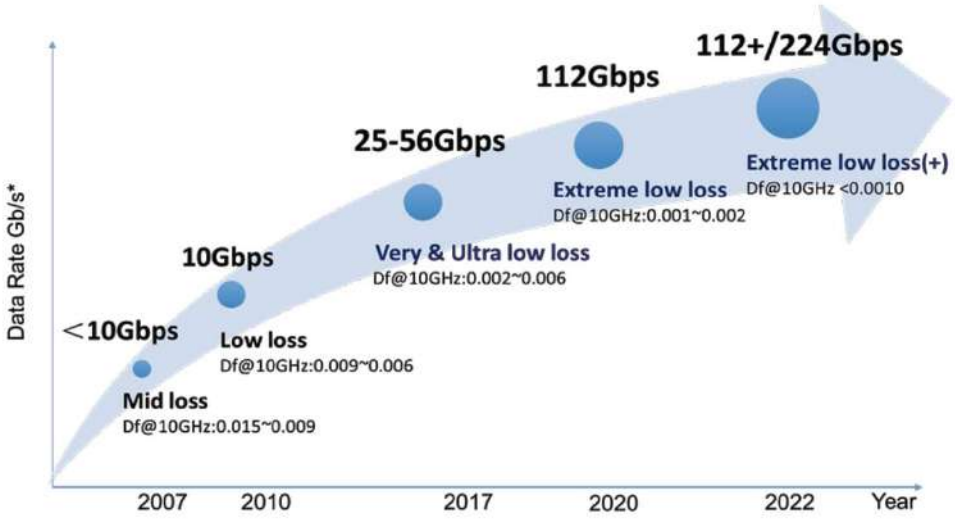
OIF CEI-224G New Project Starts (2022년 Q1)

1. Advanced Silicon/Package/PCB SI 기술동향

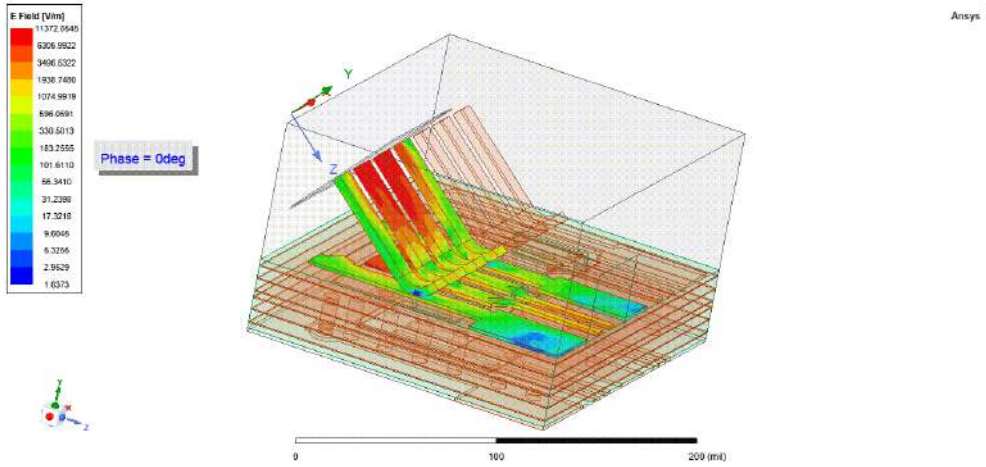
CEI-224G

- 224G 급 PCB 재질 및 커넥터 부품은 현재 샘플 수준으로 개발되어 있음. => 고도화된 채널 SI 시뮬레이션 및 칩의 고도화된 DFE 포함 Eye 시뮬레이션을 결합하여 설계 가능하여야 하며, 도달 거리를 늘리기 위해 SI 설계 능력 및 시뮬레이션 환경이 필수적임.

- 휴윈은 국내뿐 아니라 세계 최고 수준의 채널 SI 시뮬레이션 및 측정 (~100GHz) 관련 기술을 보유하고 있으며, 국내 뿐 아니라 세계 최고 수준의 채널 SI 검증 소프트웨어 엔진을 보유하고 있음. => 정부지원 과제를 통해 200Gbps 급 전용 검증 소프트웨어(PAM4/PAM8 채널 뷰) 를 추가로 개발 추진중임.



PCB High-Speed Material Evolution



224G 채널 설계에는 3D EM 해석 및 설계 기술이 매우 중요함.

2. 시뮬레이션 통한 SI 설계

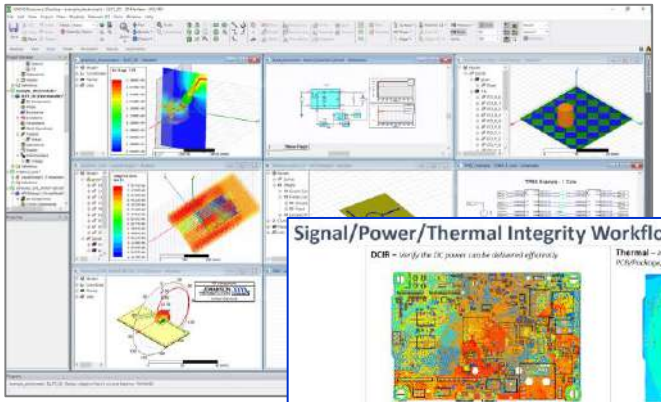
ANSYS Electronics Enterprise

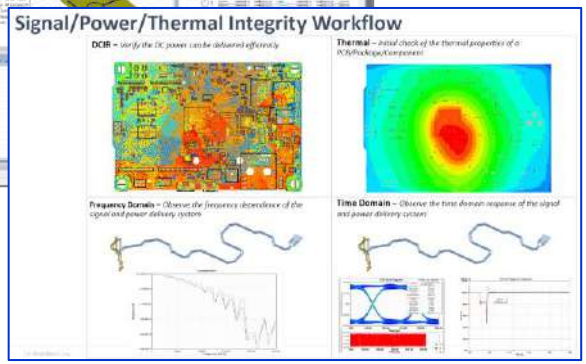
3D EM 모델링/분석 및 PCB SI/PI :

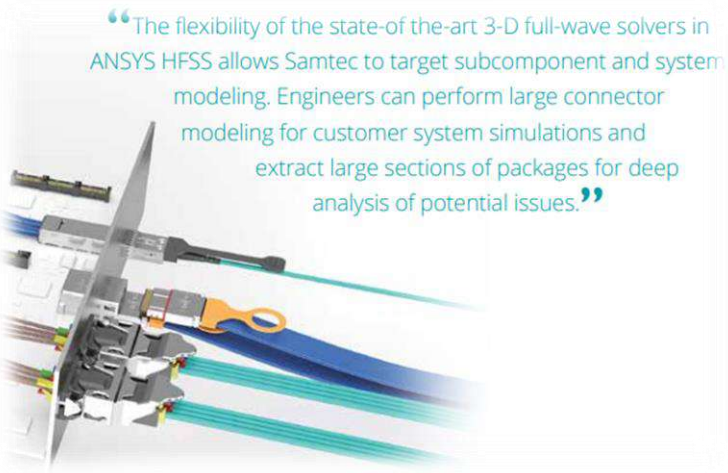
ANSYS Electronics Enterprise :

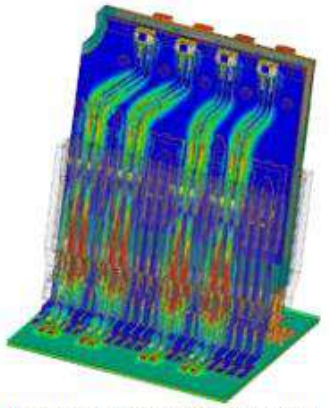
=> Electronics 분석 위한 통합 UI 및 Solvers 패키지

- 3D EM : HFSS(High Freq.), Maxwell(Low Freq.)
- PCB EM SI/PI : SIwave
- RLC Extraction : Q3D Extractor
- Thermal : Icepak
- Circuit

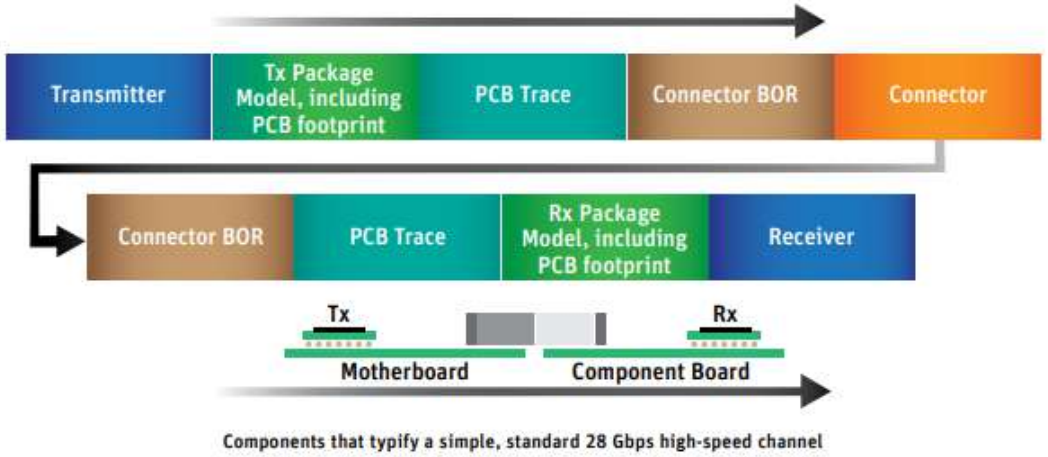








ANSYS HFSS-modeled electric field within Samtec MEC5-DV connector and cable assembly



Components that typify a simple, standard 28 Gbps high-speed channel

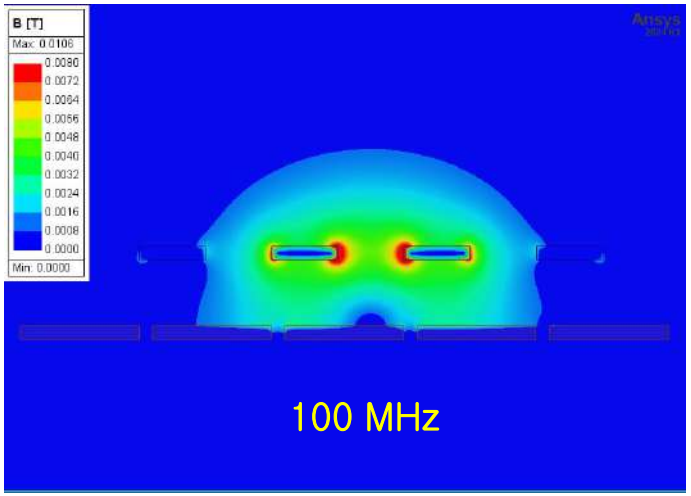
Source : **"Deep Channel Analysis for High-Speed Interconnect Solutions", Ansys Advantage 2017**

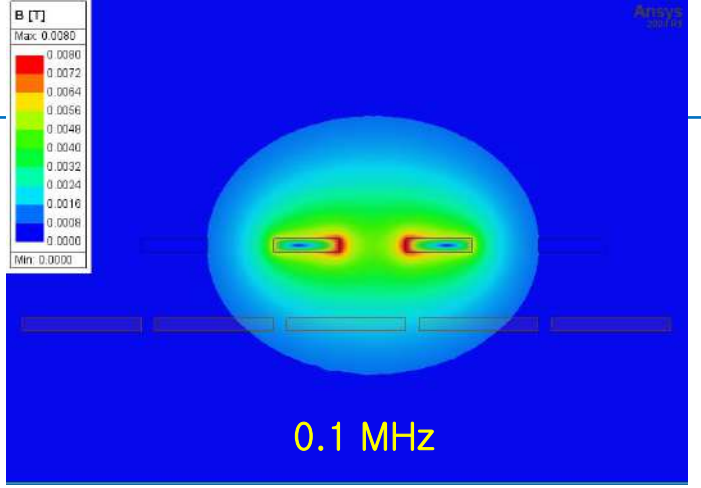
2. 시뮬레이션 통한 SI 설계

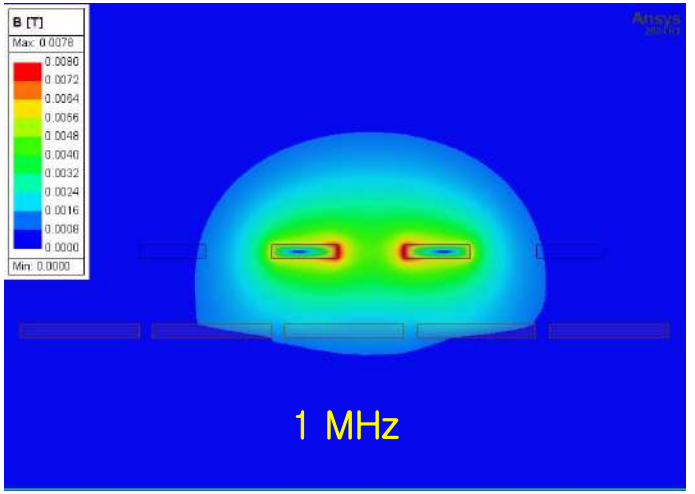
Standard PCB : ~100um width/space

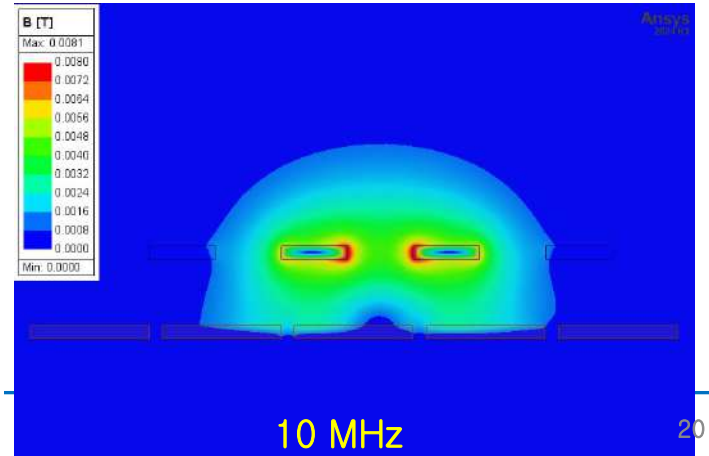
일반 PCB 패턴의 경우

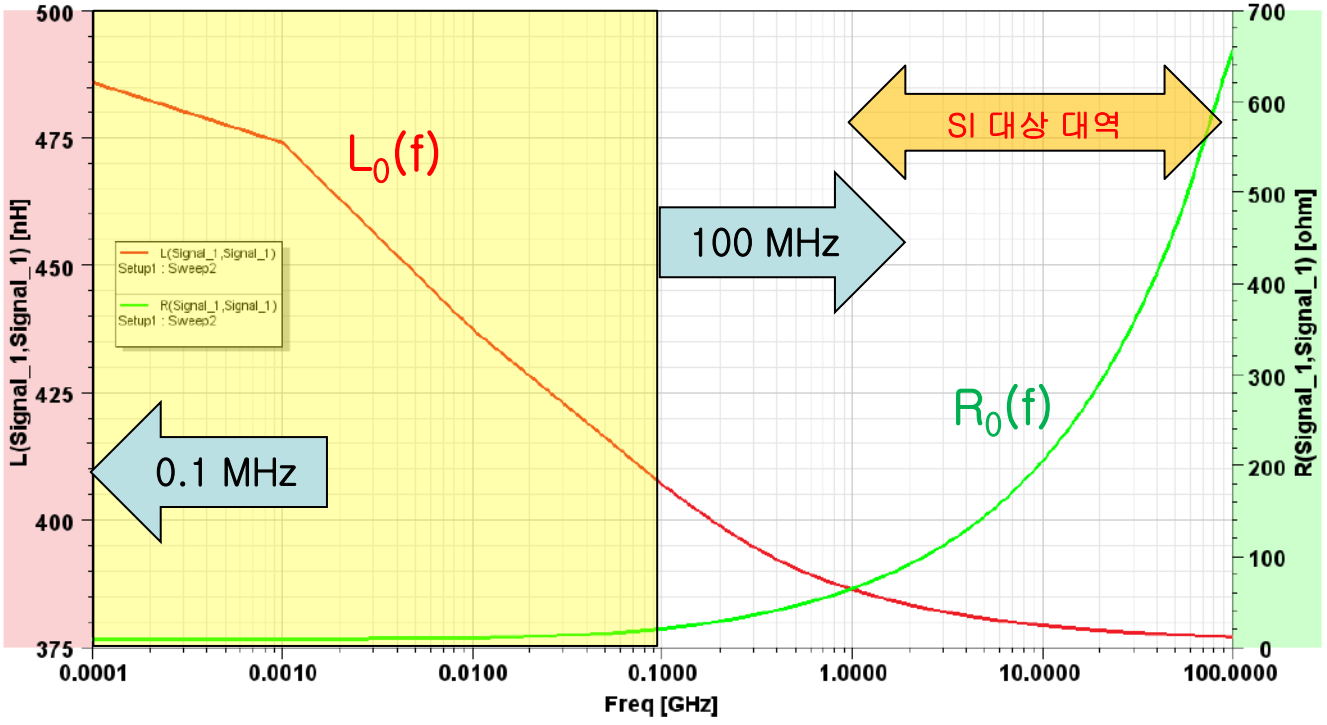
- 0.1~100MHz Ldc -> Lac
- 1GHz : 40ohm/meter 저항









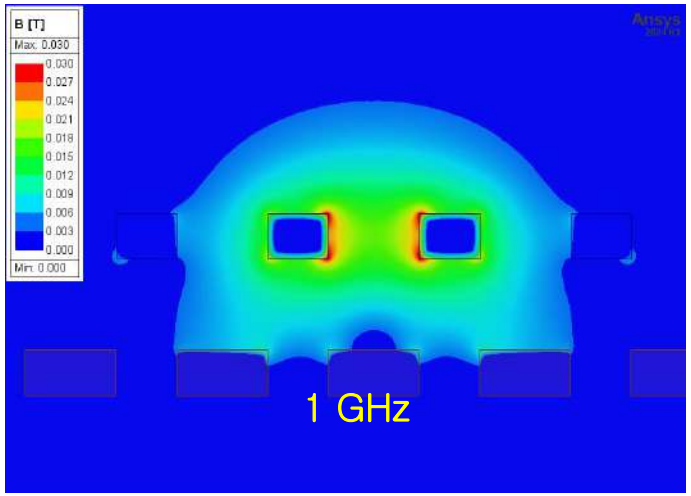


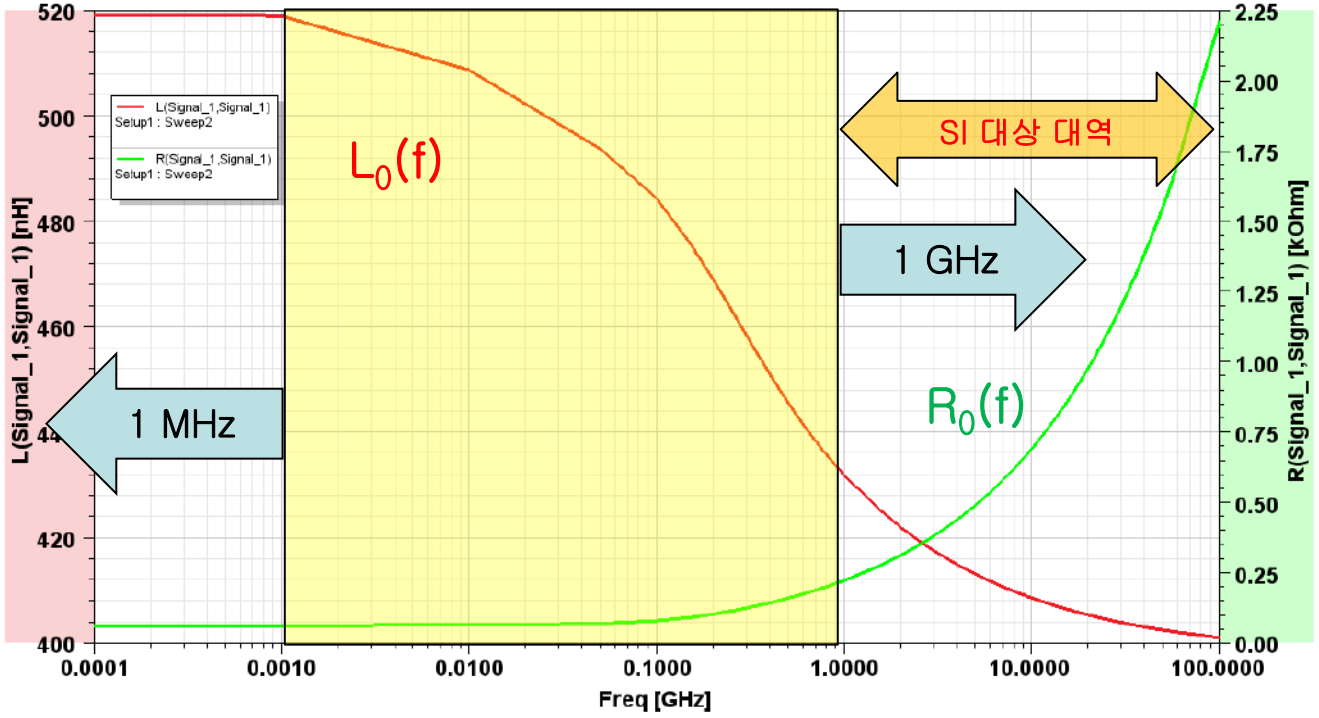
2. 시뮬레이션 통한 SI 설계

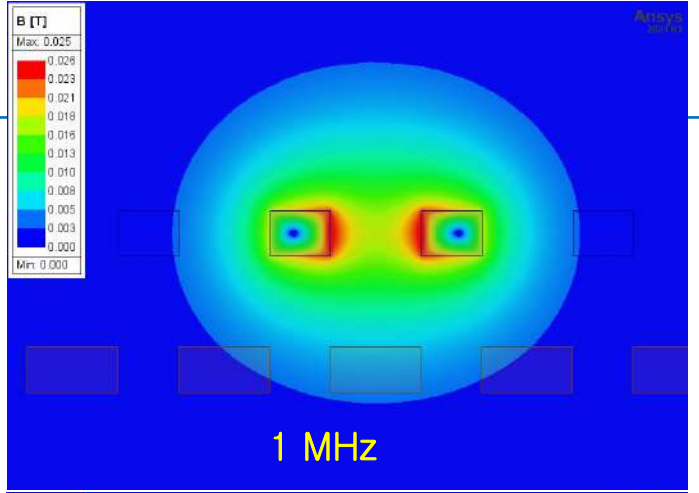
Standard PKG : <50um width/space

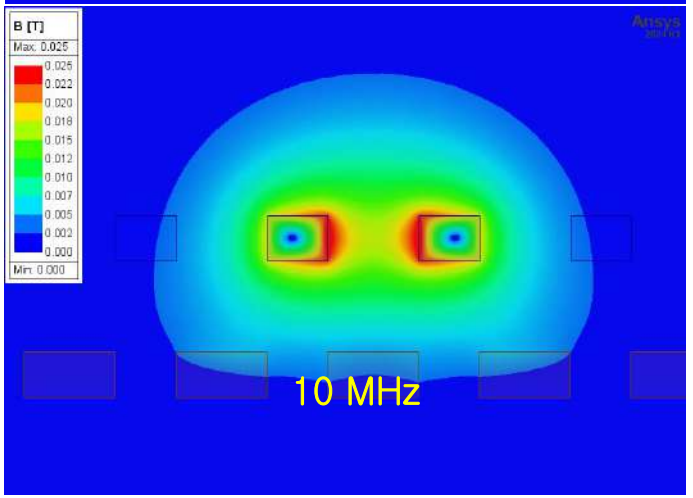
일반 PKG 패턴의 경우

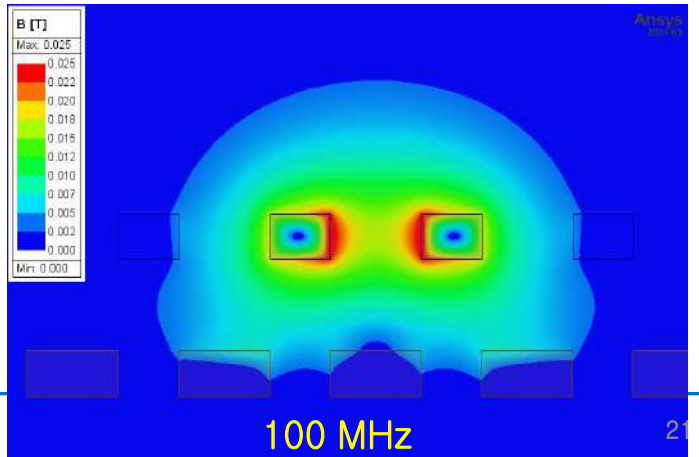
- 1~1000MHz Ldc -> Lac
- 1GHz : 25ohm/10cm 저항









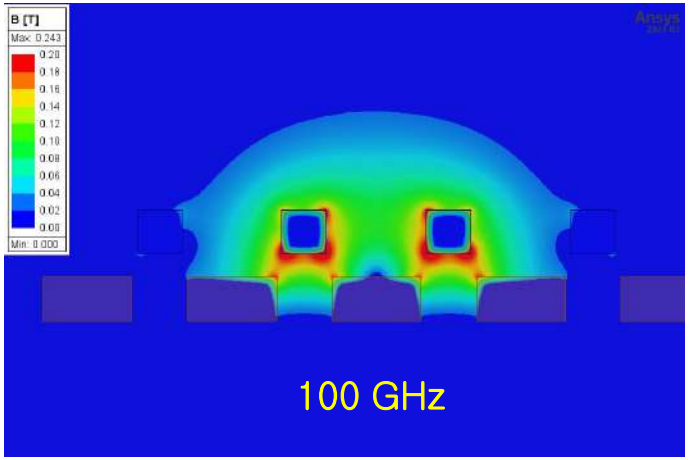


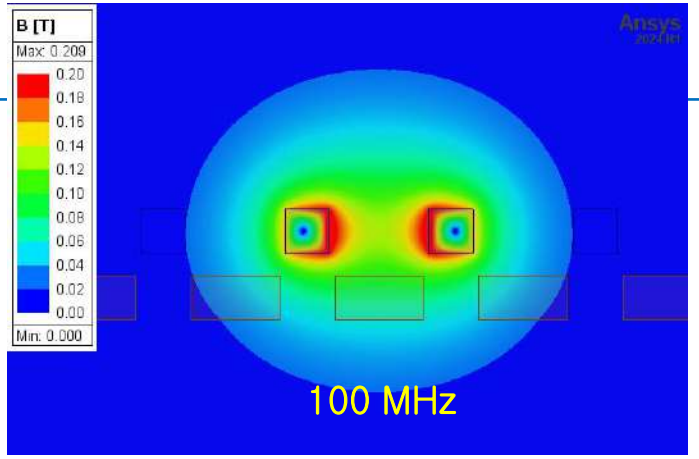
2. 시뮬레이션 통한 SI 설계

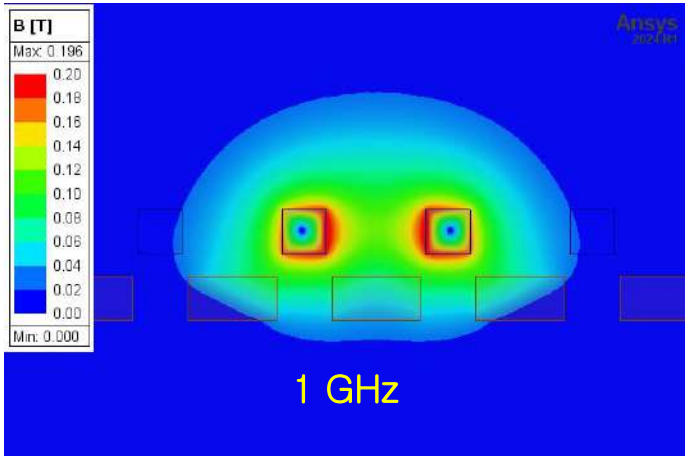
Standard Silicon Interposer : <5um width/space

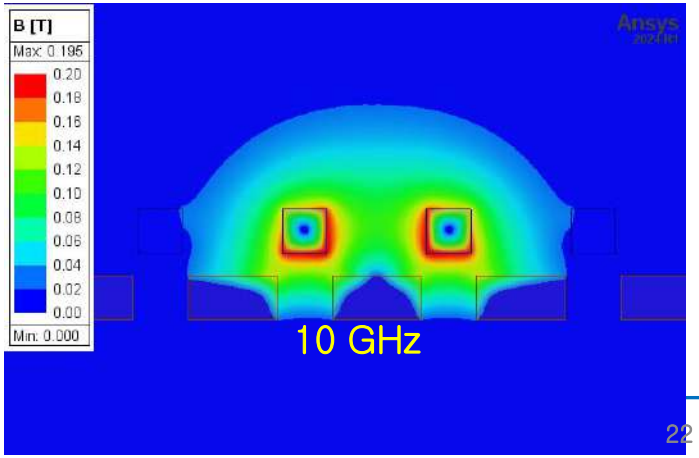
Standard Silicon Interposer 패턴의 경우

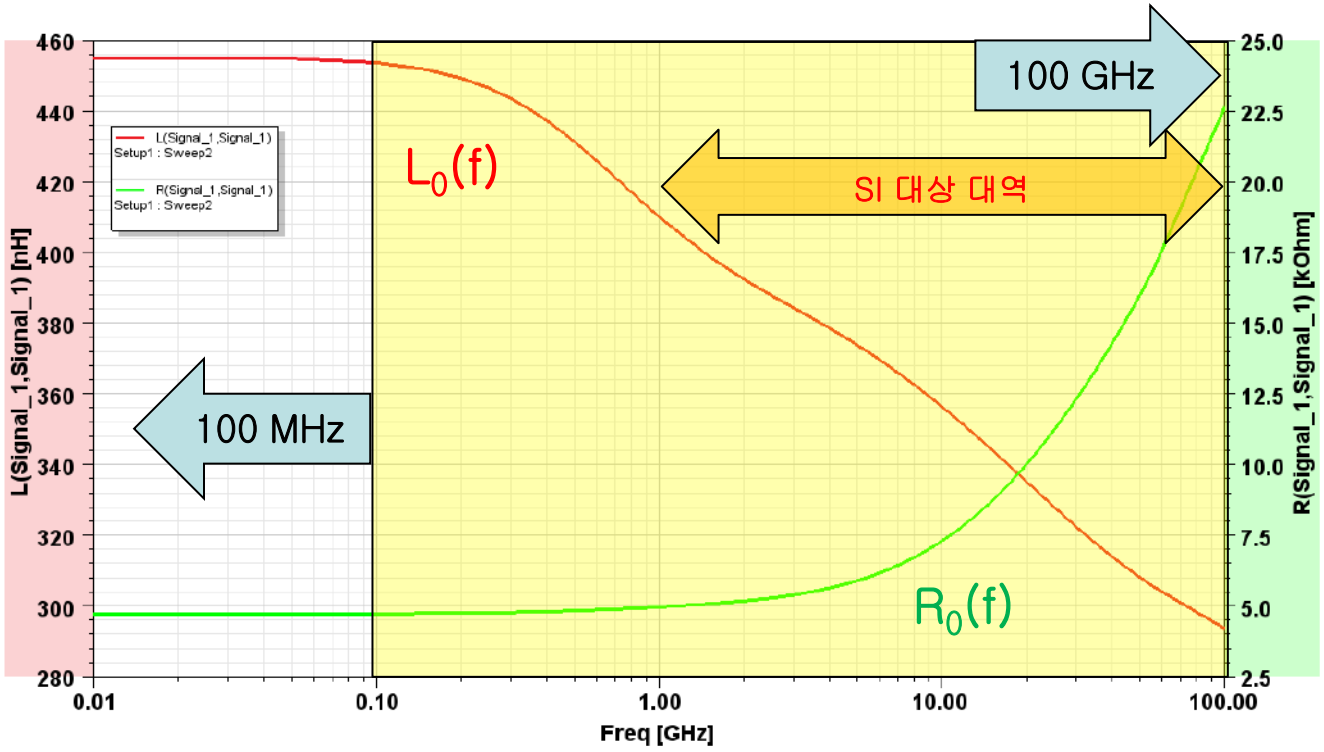
- 0.1~100GHz Ldc -> Lac
- 1GHz : 50ohm/1cm 저항









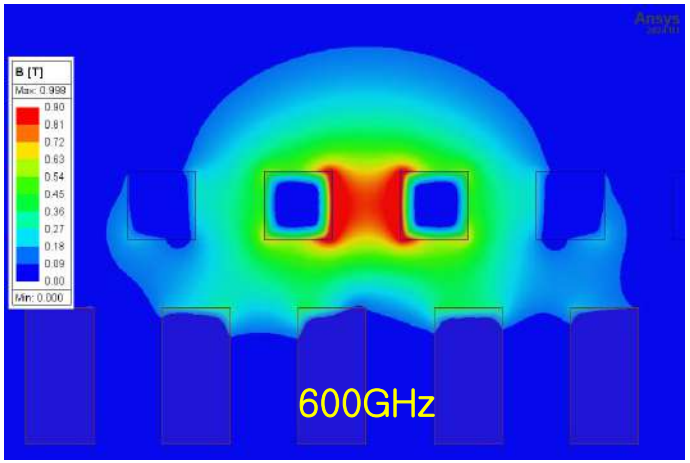


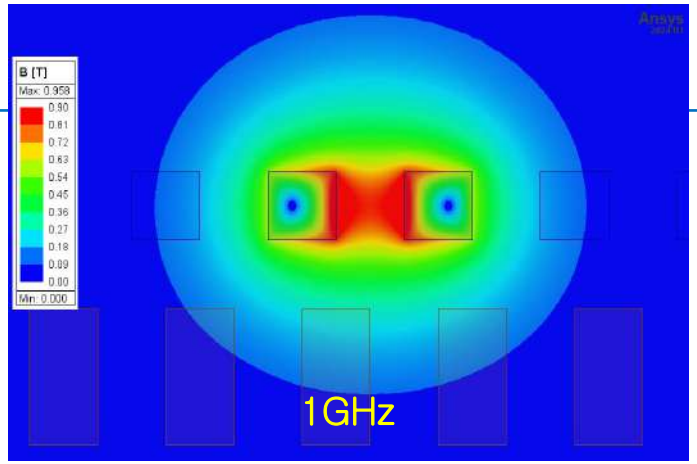
2. 시뮬레이션 통한 SI 설계

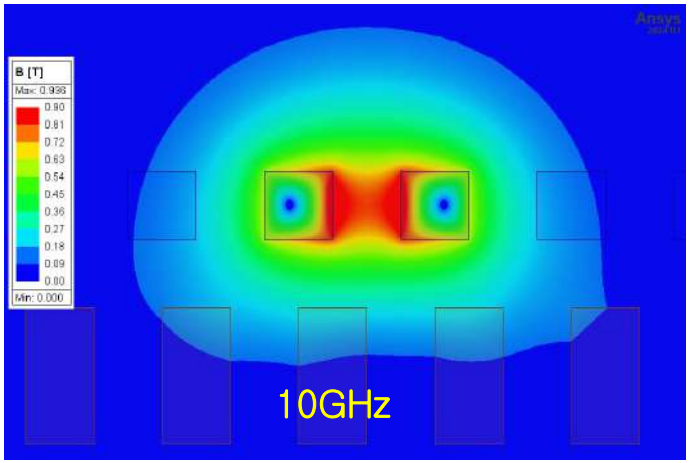
Advanced Silicon Interposer : <1um width/space

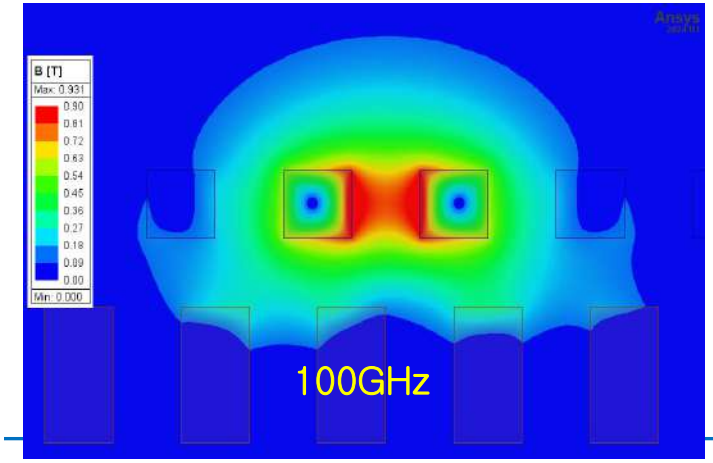
Advanced Silicon Interposer
패턴의 경우

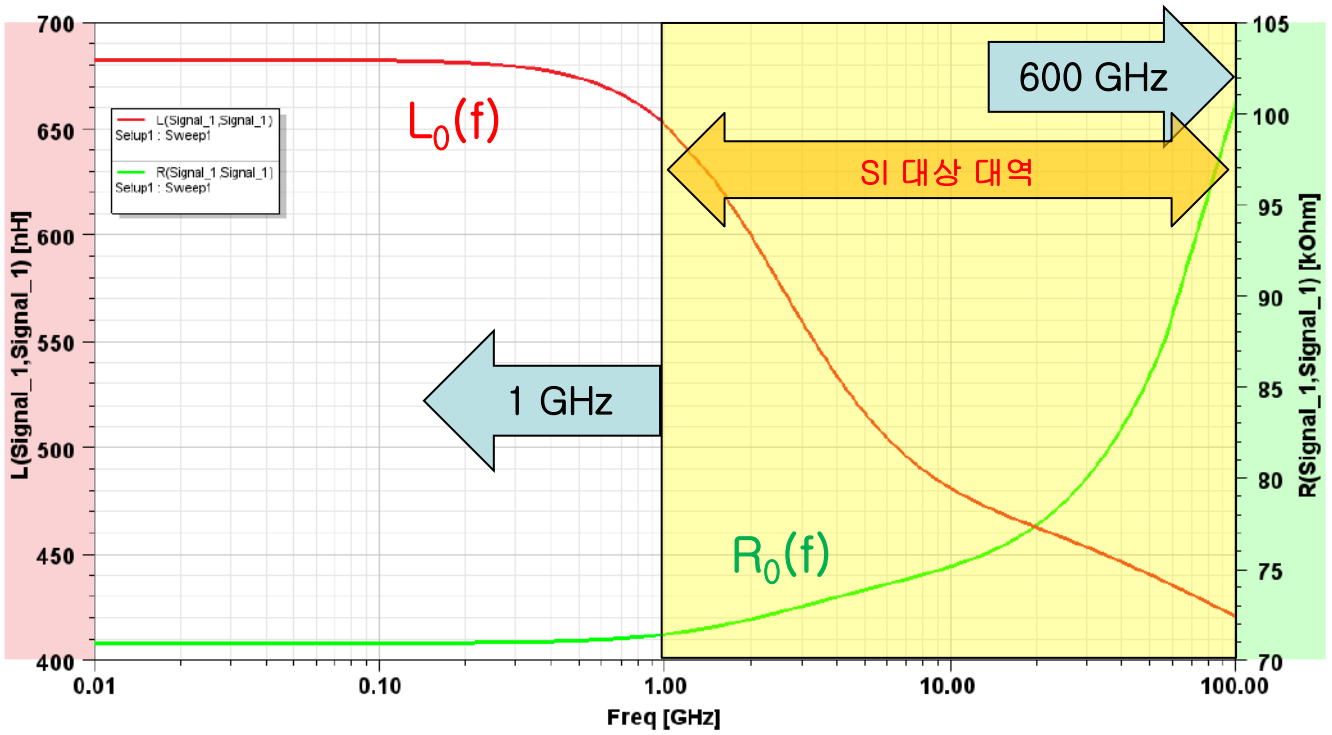
- 1~600GHz Ldc -> Lac
- 1GHz : 700 ohm/1cm 저항









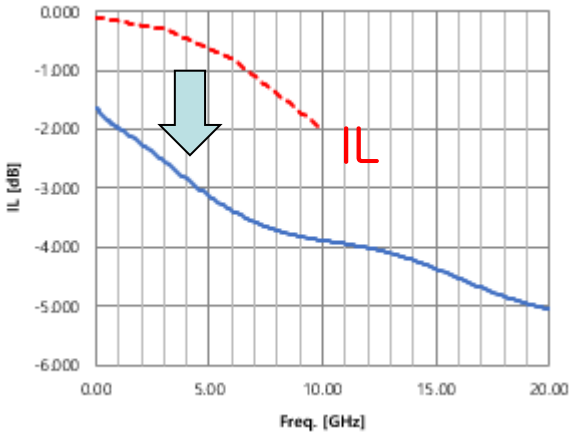


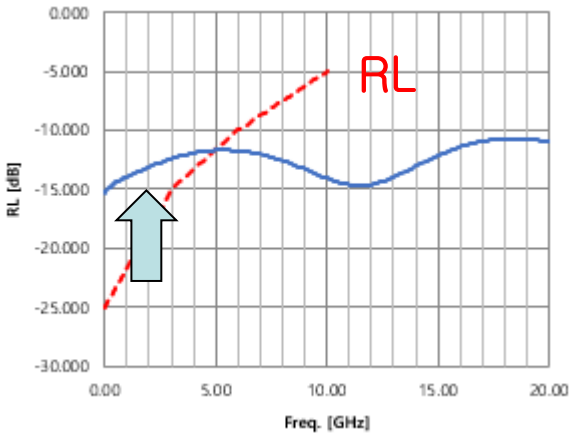
2. 시뮬레이션 통한 SI 설계

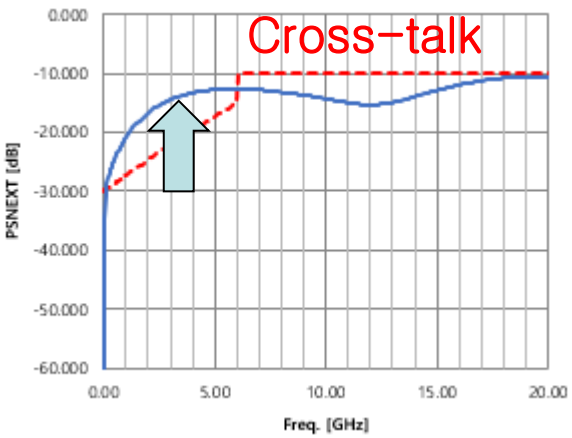
Silicon Interposer Basic SI check : IL, RL, Cross-talk, TDR, TDT

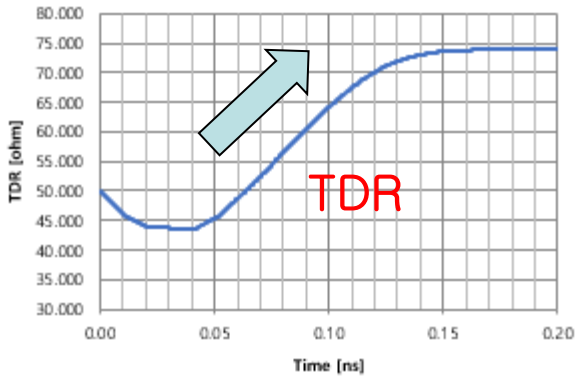
Silicon Interposer 의 경우 짧은 길이임에도 Loss 및 Cross-talk 이 큼

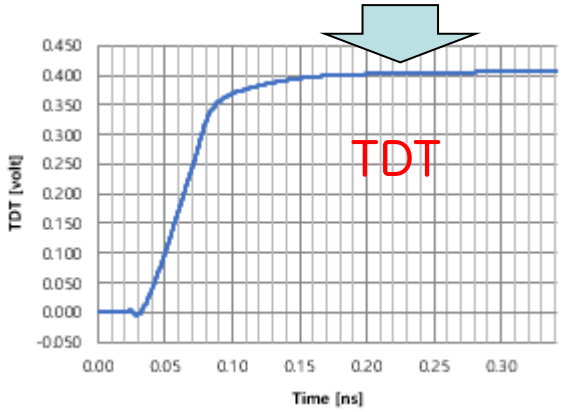
- TDR 에 R 에 의한 기울기
- TDT 에 R 에 의한 voltage DC level 감소









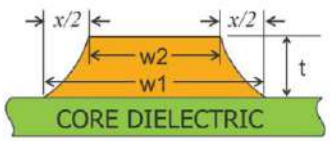


2. 시뮬레이션 통한 SI 설계

PCB Trace Etching Effect :

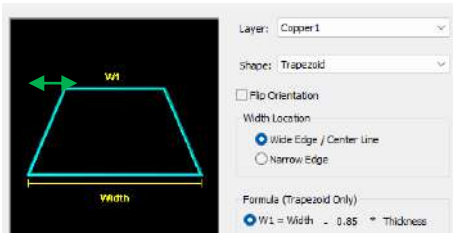
PCB Trace 설계 최적화 :

- PCB EM SI/PI : SIwave 이용 PCB Trace Impedance 확인 및 width/ space 최적화



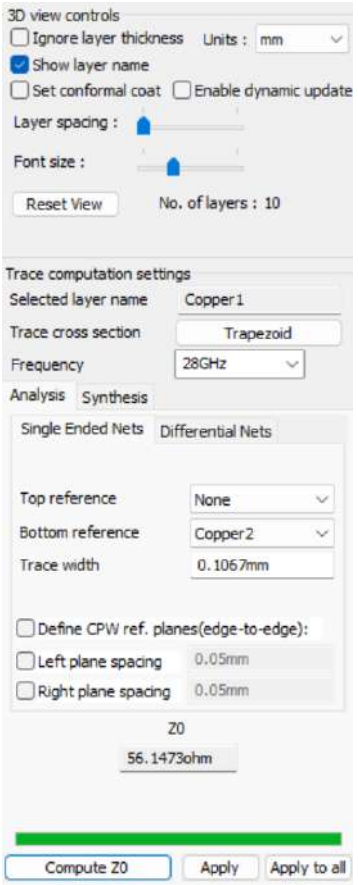
$$Etchback\ (x) = w1 - w2$$

$$Etch\ Factor\ (F) = \frac{w1 - w2}{t}$$

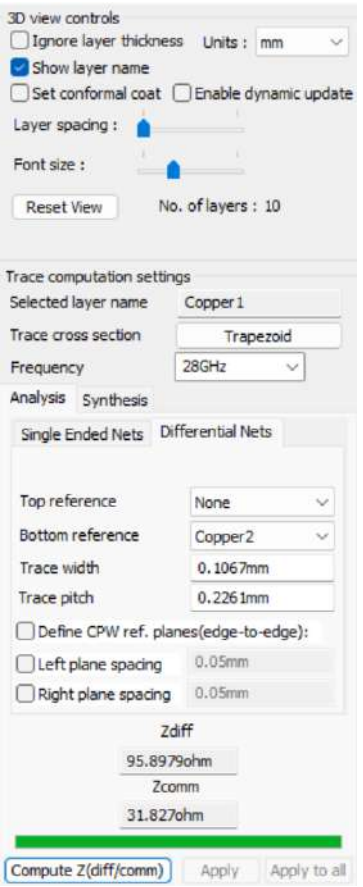


$w2 = w1 - Etch\_Factor * t$

* Etch Factor 적용시 PCB trace 의 Impedance 가 ~5옴 정도 영향을 받으므로 PCB 공정의 parameter 를 적용하여 PCB trace 의 impedance 를 확인 및 설계 시 trace width 와 space 의 최적 값을 적용함.



Single ended Z0

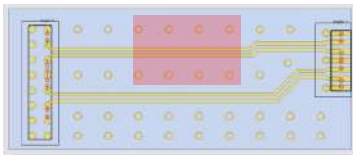


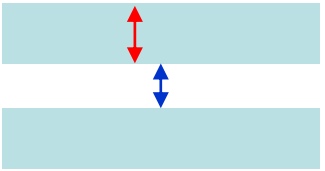
Differential Z0

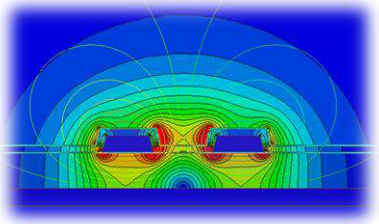
PCB Trace design issues

* PCB trace 의 공정 편차 고려하여 정확한 Impedance 설계로 튜닝

a, b, c 설계 변수 -> SIwave 이용 Trace 분석 후 정확한 Z0 값 튜닝 필요



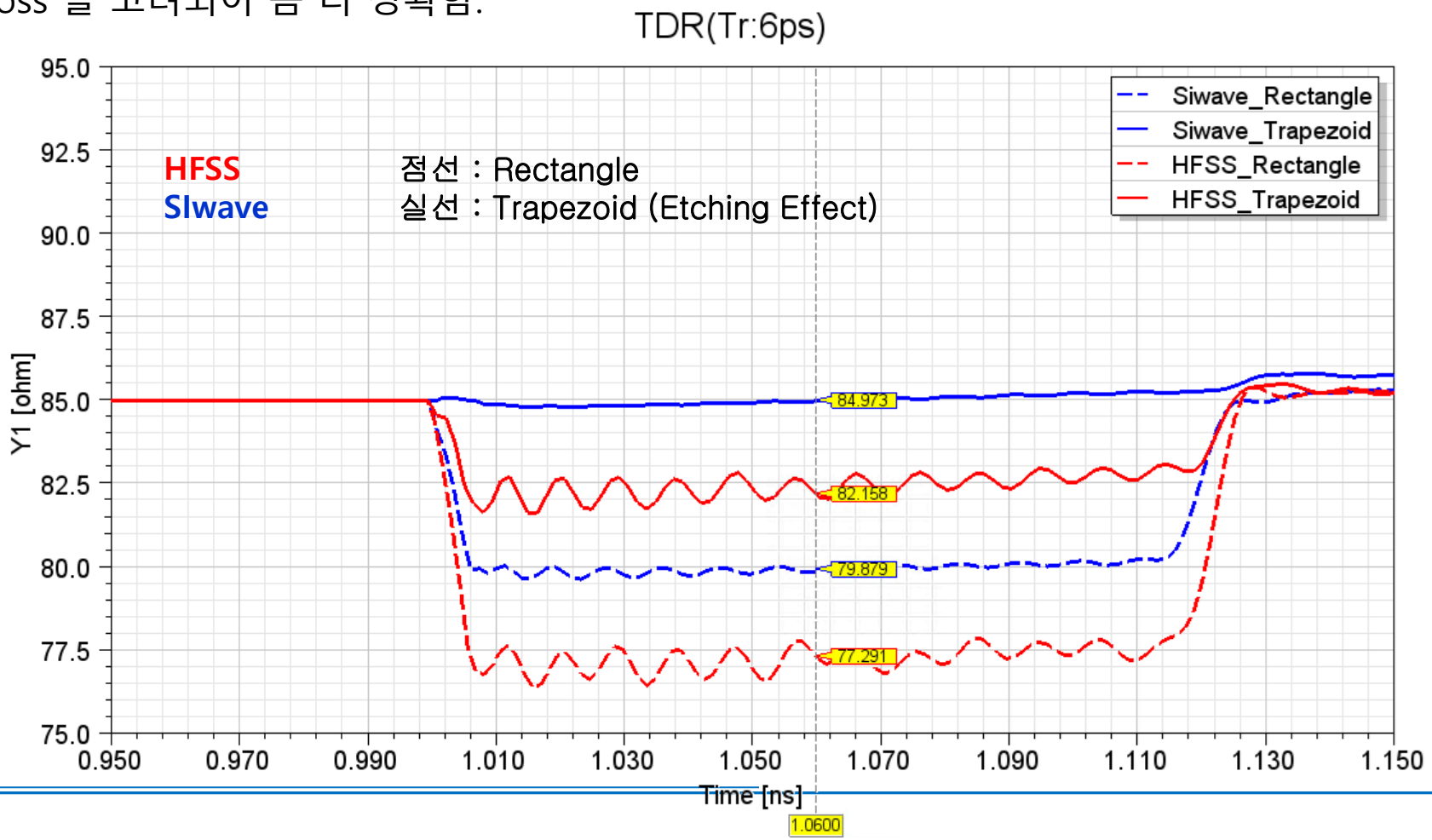




PCB Trace Etching Effect :

PCB Trace 설계 최적화 :

- ❖ PCB Etching Effect 에 의해 5ohm정도 TDR Impedance 차이 남
- ❖ Etching 고려한 상태에서 SIwave는 약 85ohm, HFSS는 약 82ohm를 나타냄 => HFSS 가 radiation loss 를 고려되어 좀 더 정확함.

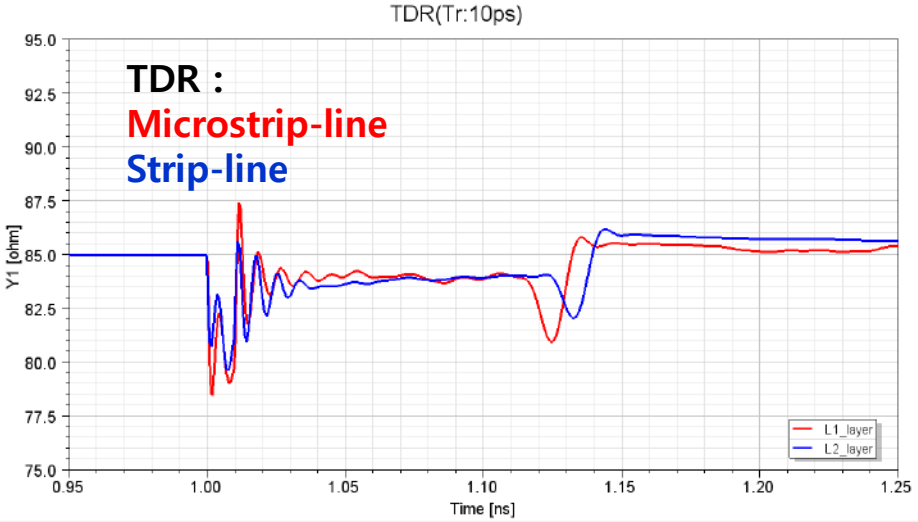


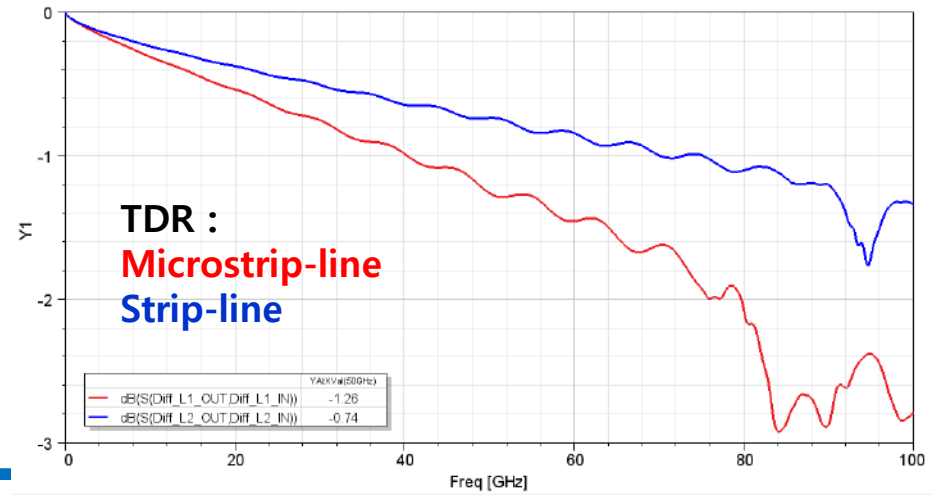
2. 시뮬레이션 통한 SI 설계

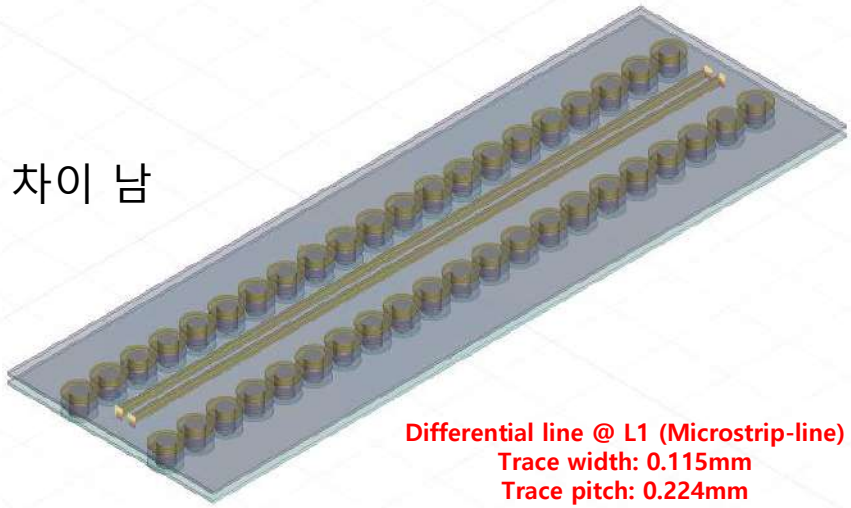
PCB Trace : Microstrip-line vs. Strip-line

PCB Trace (Microstrup-line vs. Strip-line) : HFSS 분석

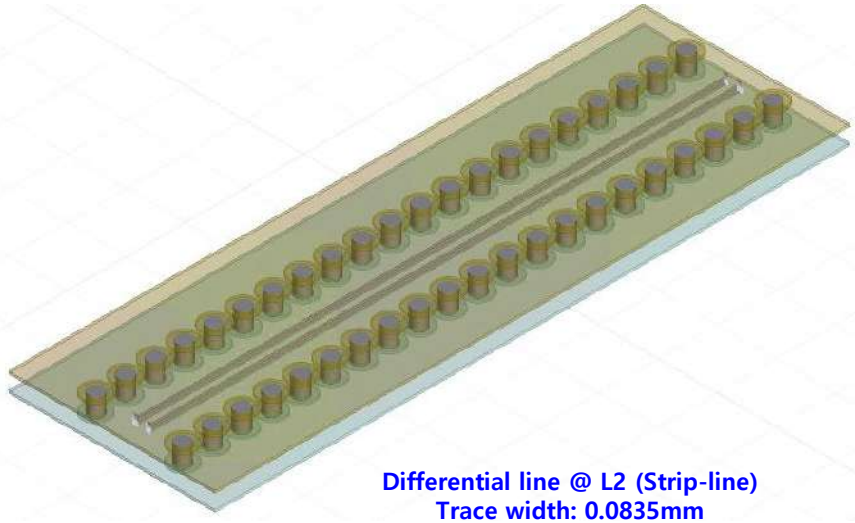
❖ Microstrip 과 Strip 의 경우 TDR 동일, delay 및 loss 가 차이 남







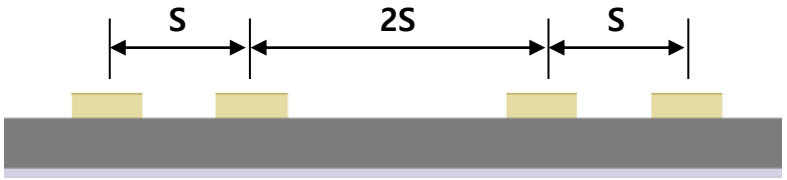
Differential line @ L1 (Microstrip-line)
Trace width: 0.115mm
Trace pitch: 0.224mm



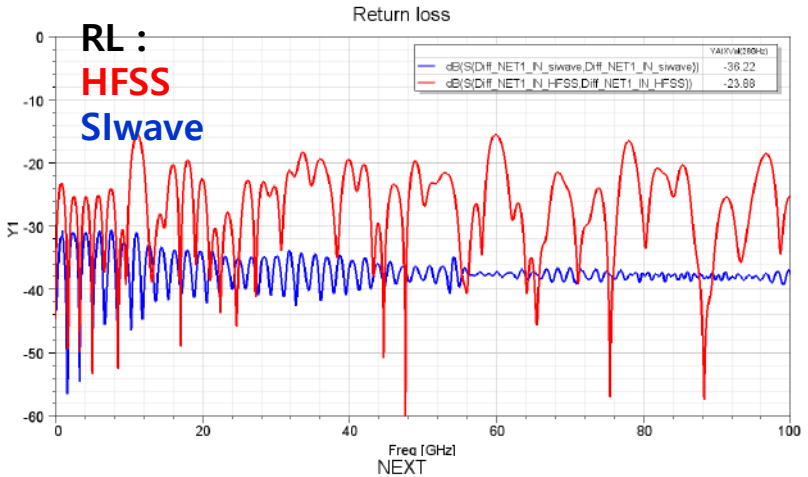
Differential line @ L2 (Strip-line)
Trace width: 0.0835mm
Trace pitch: 0.224mm

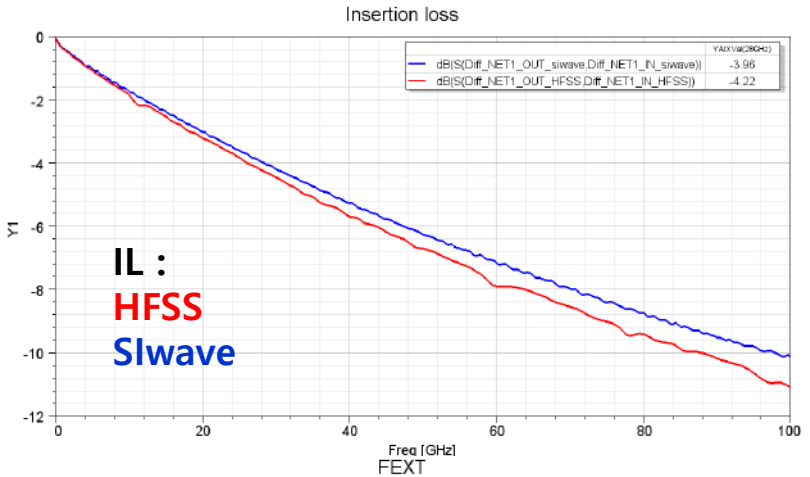
PCB Trace, Differential line 의 Cross talk : SIwave vs. HFSS

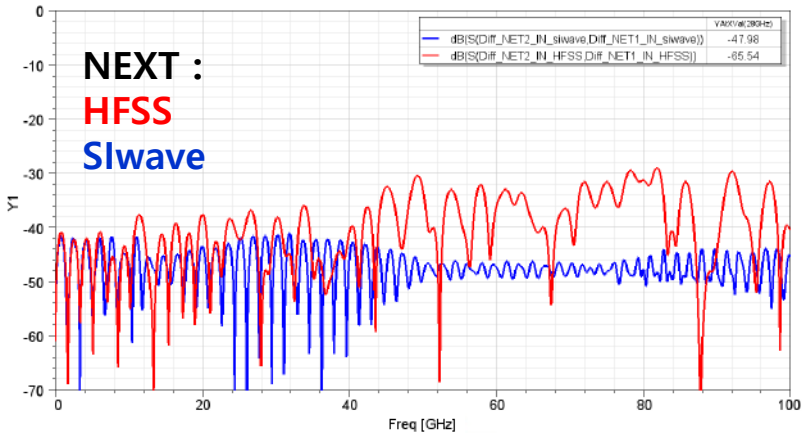
PCB Trace (Differential line) : SIwave vs. HFSS 비교

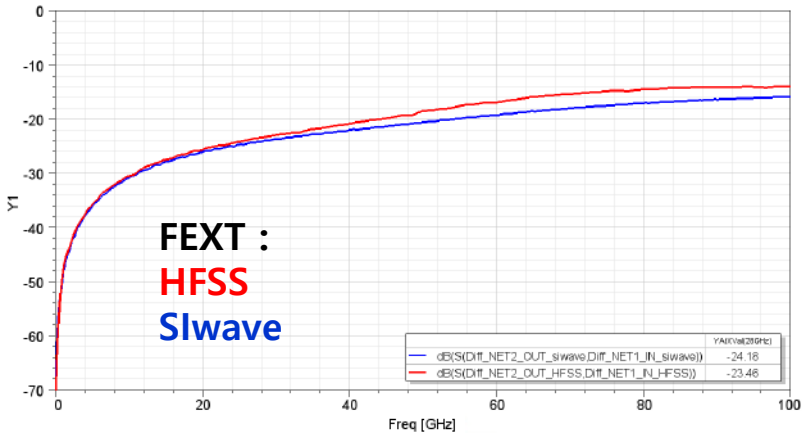


❖ Trace 간 cross-talk 및 IL, RL 은 SIwave 와 HFSS 결과 유사함.
=> Trace 구간은 SIwave 로, Via 등 구간은 HFSS 로 Hybrid 분석 가능









2. 시뮬레이션 통한 SI 설계

PCB Connector Pad Effect :

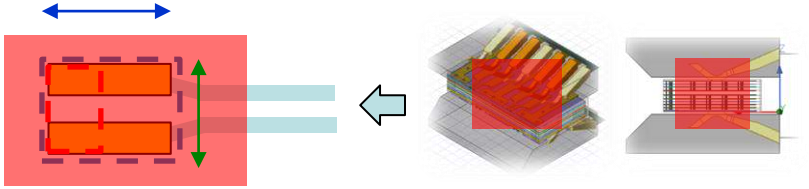
Connector-PCB interconnect 설계 최적화 :

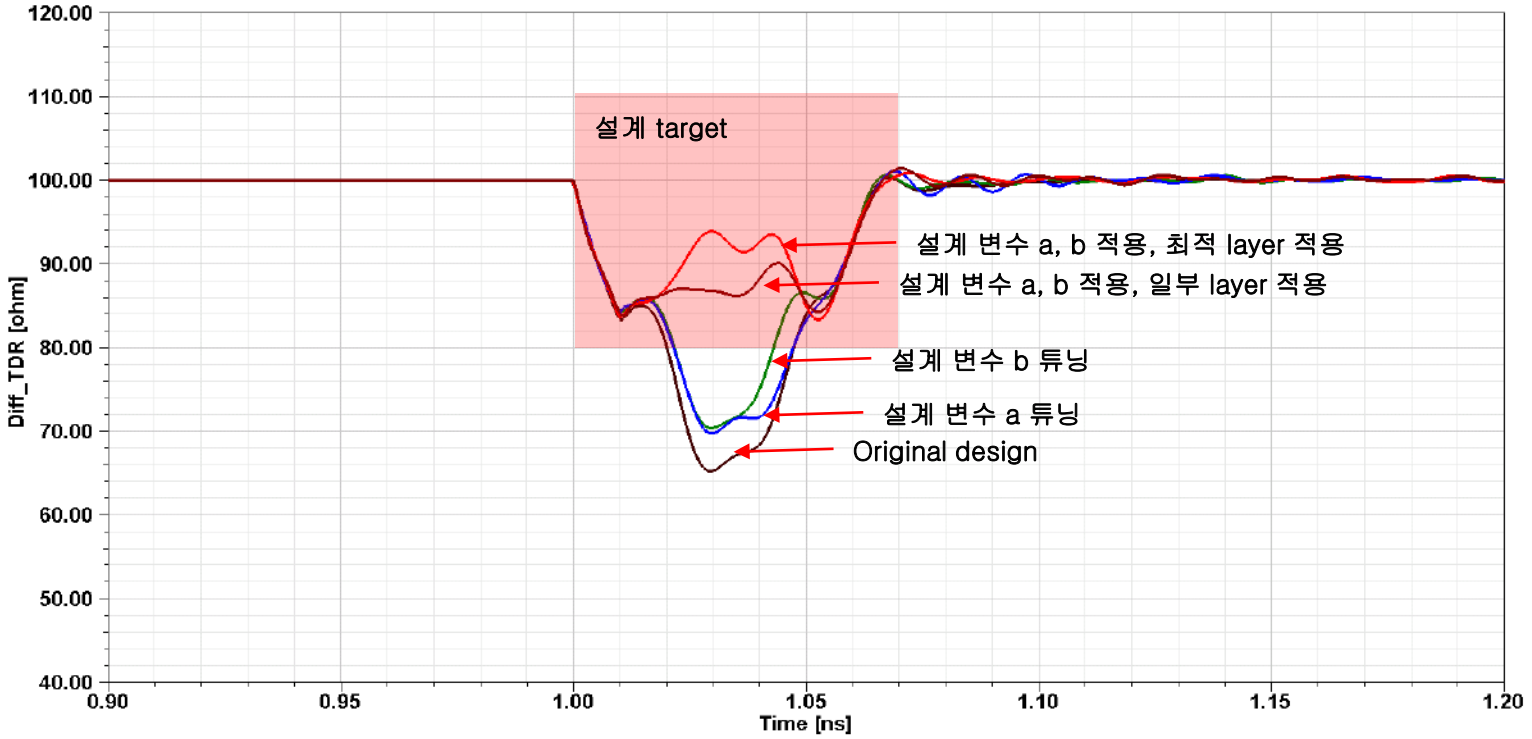
- 3D EM : HFSS(High Freq.) 이용 Connector pad 부분 TDR impedance 최적화

Connector – PCB interconnect design issues

* Pad contact 에 의한 stub, pad 부분 impedance, Ground reference plane 의 void 설계 등 최적화 필요함.

a, b, c 설계 변수 -> 0.1mm 단위로 3D EM 분석 후 TDR 확인하여 최적화 튜닝 필요



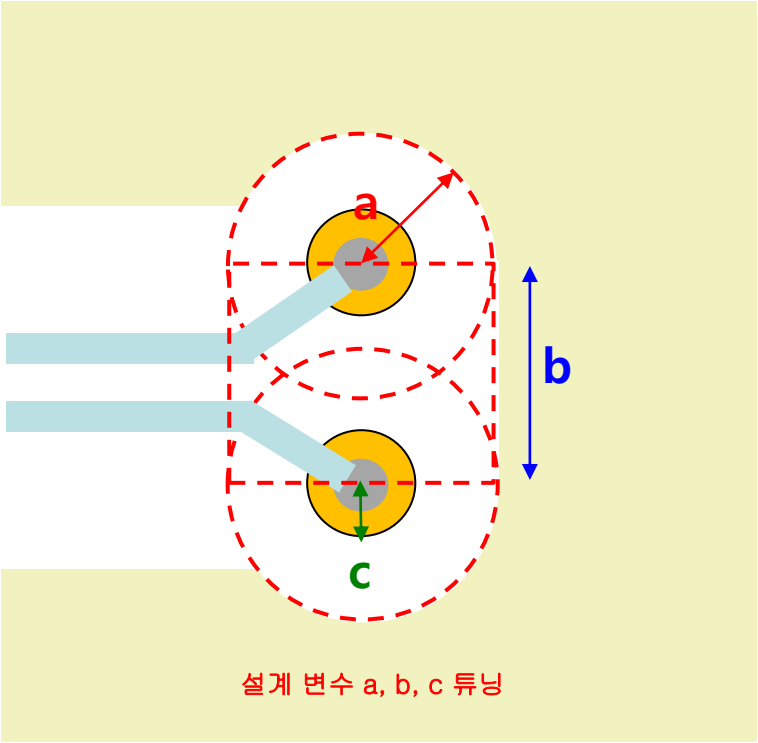


2. 시뮬레이션 통한 SI 설계

Via Pad, Antipad Effect :

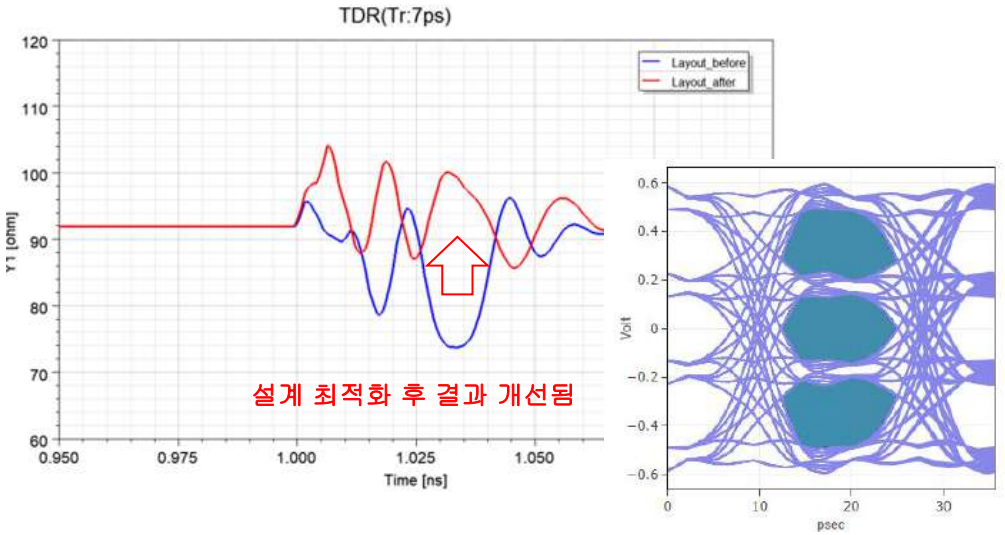
Via interconnect 설계 최적화 :

- 3D EM : HFSS(High Freq.) 이용 Via 부분 TDR impedance 최적화



PCB via design issues

* via size 및 anti pad 설계에 의한 TDR Impedance 튜닝 필요함.

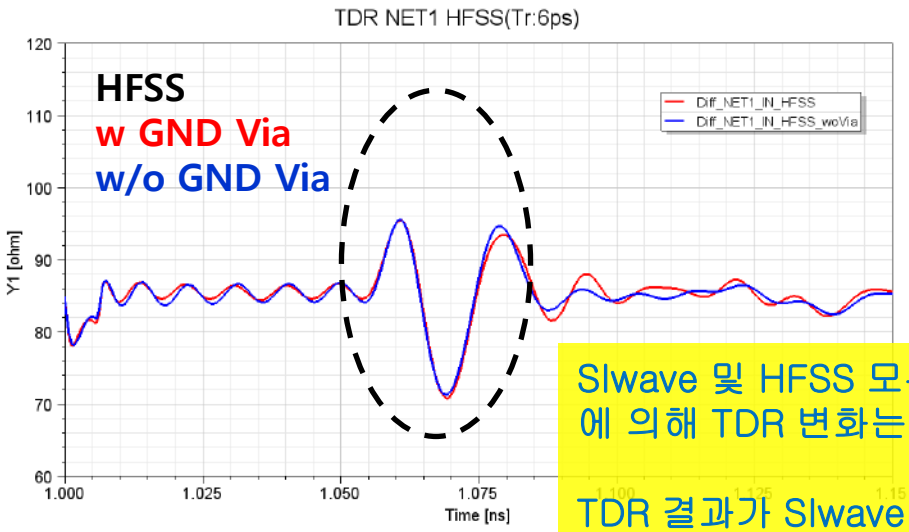


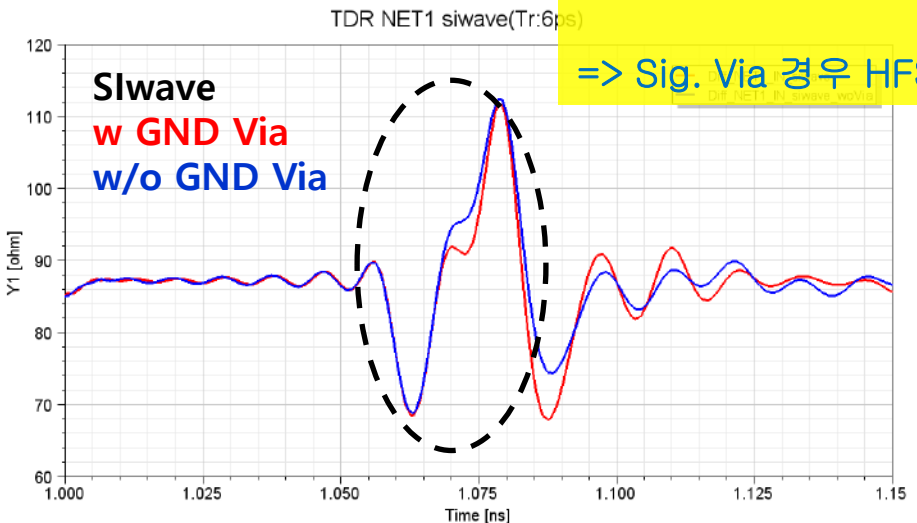
2. 시뮬레이션 통한 SI 설계

Sig. Via 주변 GND Via 영향 분석 :

Sig. Via 주변 GND via 에 의한 TDR (SIwave vs. HFSS) :

- 3D EM : HFSS(High Freq.) 이용 분석 : 5시간 (32cores, 512GB RAM)

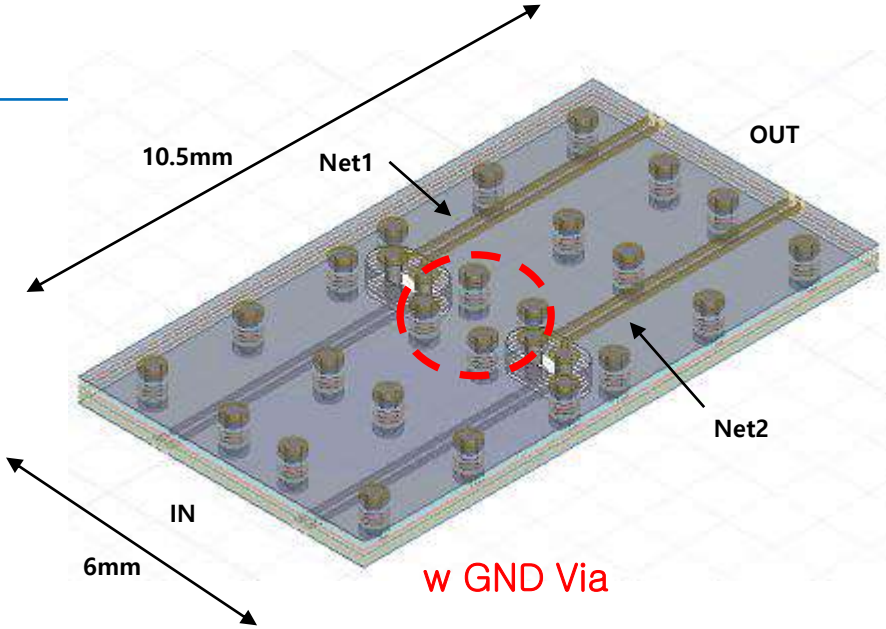


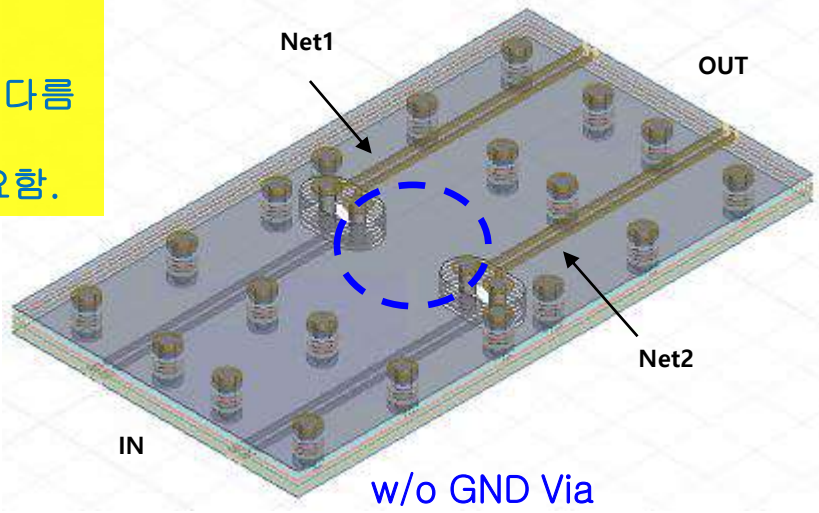


SIwave 및 HFSS 모두 주변 GND via 에 의해 TDR 변화는 없음.

TDR 결과가 SIwave 와 HFSS 가 다름

=> Sig. Via 경우 HFSS 분석 필요함.



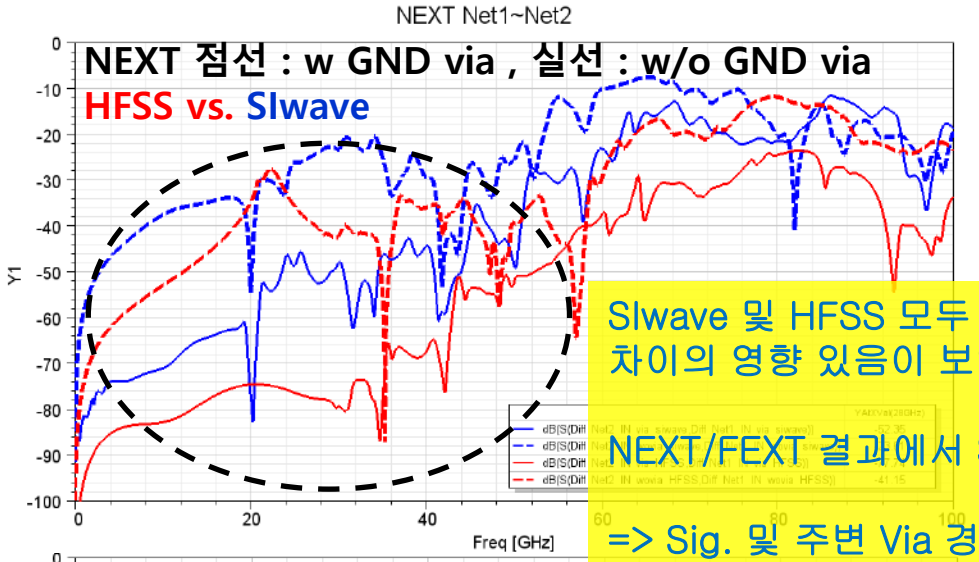


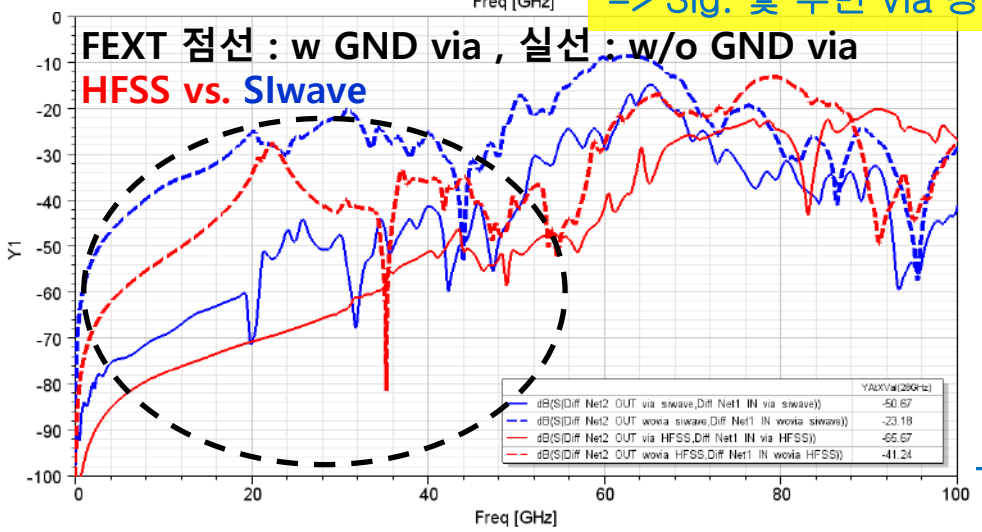
2. 시뮬레이션 통한 SI 설계

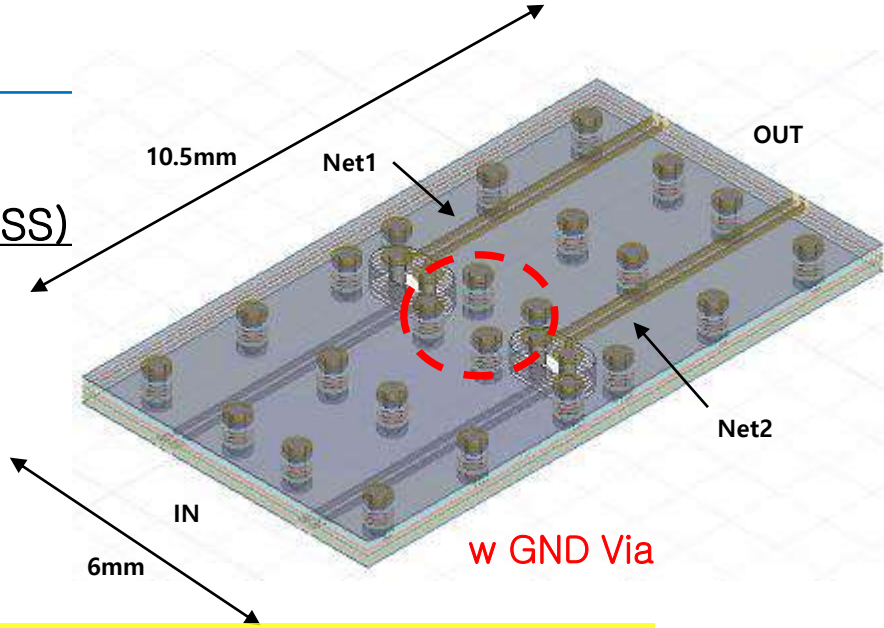
Sig. Via 주변 GND Via 영향 분석 :

Sig. Via 주변 GND via 에 의한 NEXT/FEXT (SIwave vs. HFSS)

- 3D EM : HFSS(High Freq.) 이용 분석 : 5시간 (32cores, 512GB RAM)



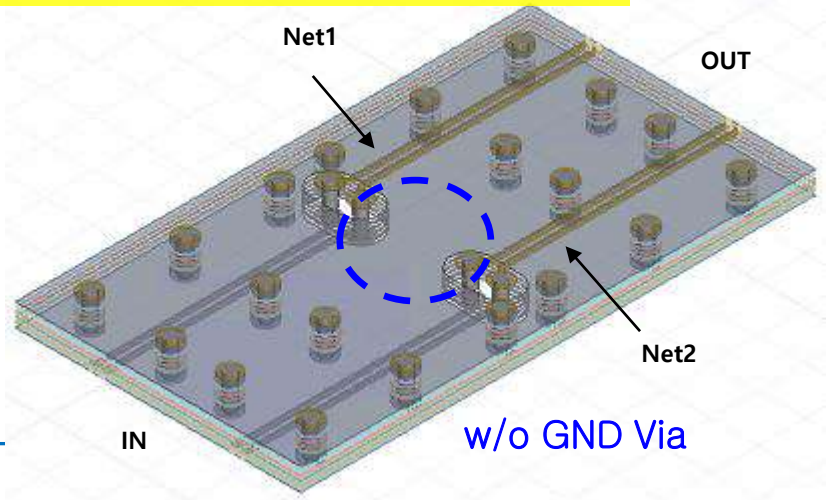




SIwave 및 HFSS 모두 주변 GND via 에 의해 Cross Talk => 약 25dB 차이의 영향 있음이 보임.

NEXT/FEXT 결과에서 SIwave 가 HFSS 보다 10dB정도 크게 반영됨.

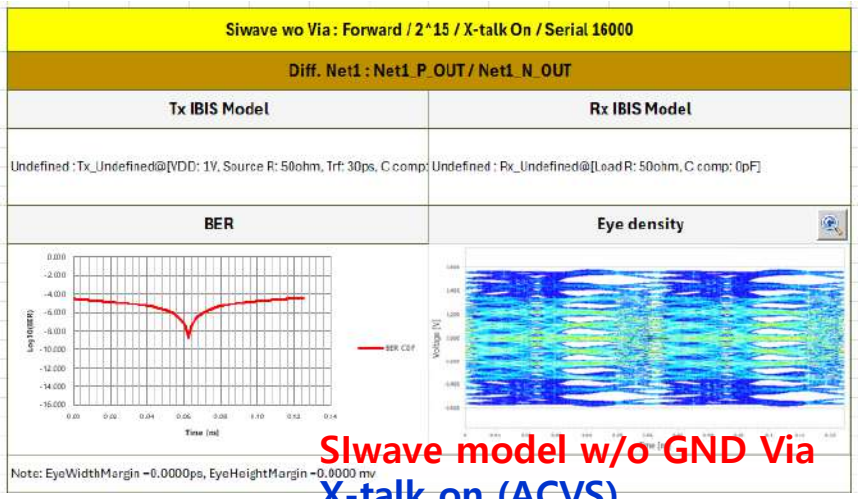
=> Sig. 및 주변 Via 경우 HFSS 분석 필요함.



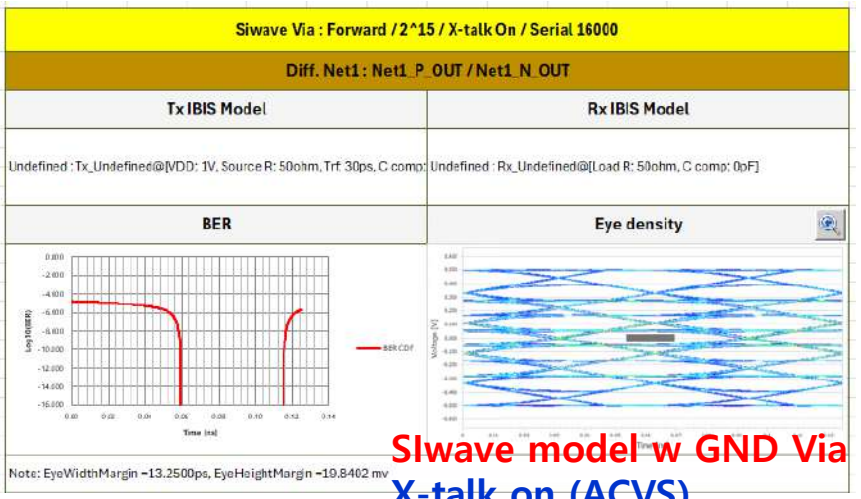
2. 시뮬레이션 통한 SI 설계

Sig. Via 주변 GND Via 영향 분석 :

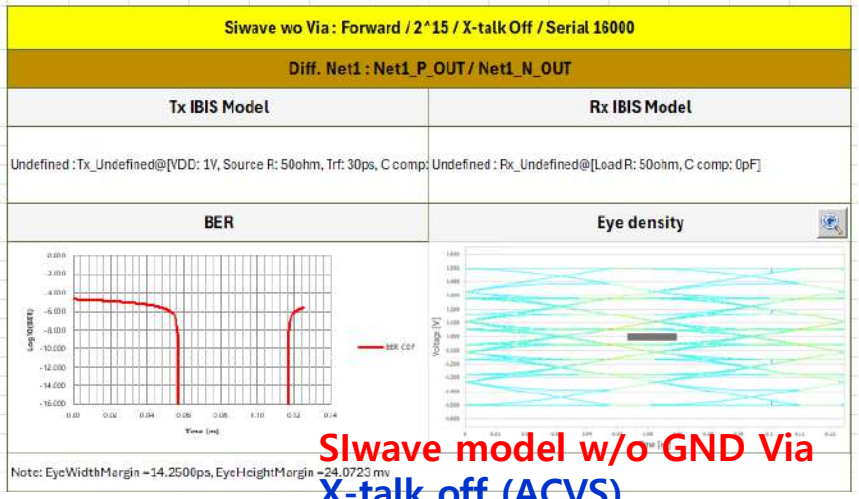
Sig. Via 주변 GND via 에 의한 NEXT/FEXT => SIwave 모델 이용시 Eye/BER 결과



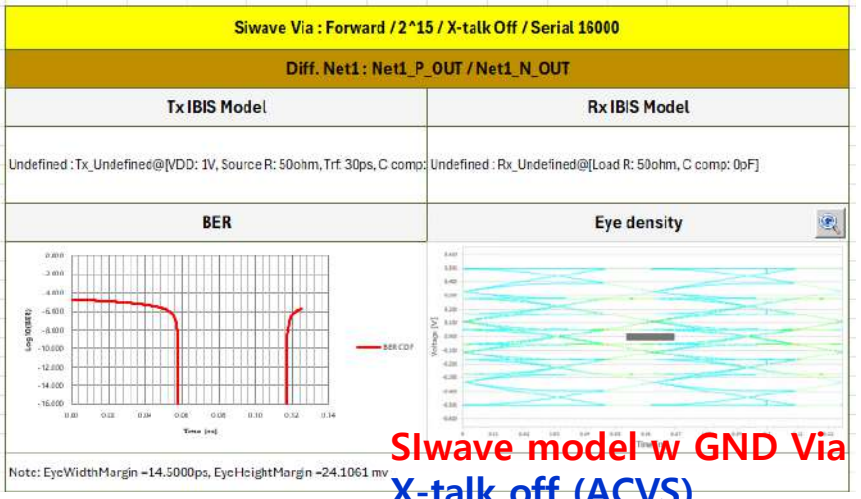
SIwave model w/o GND Via
X-talk on (ACVS)



SIwave model w GND Via
X-talk on (ACVS)



SIwave model w/o GND Via
X-talk off (ACVS)

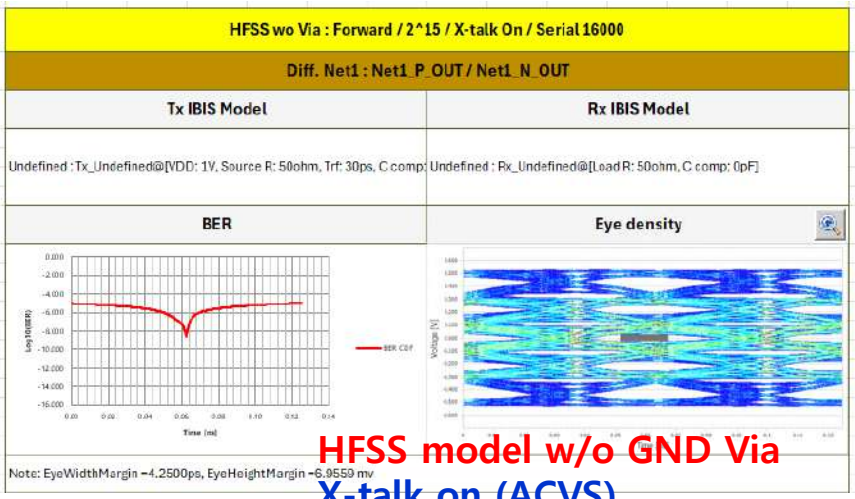


SIwave model w GND Via
X-talk off (ACVS)

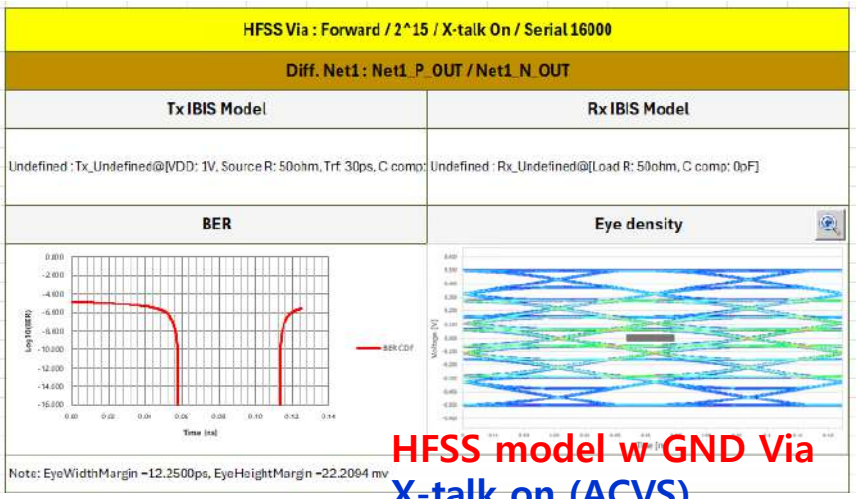
2. 시뮬레이션 통한 SI 설계

Sig. Via 주변 GND Via 영향 분석 :

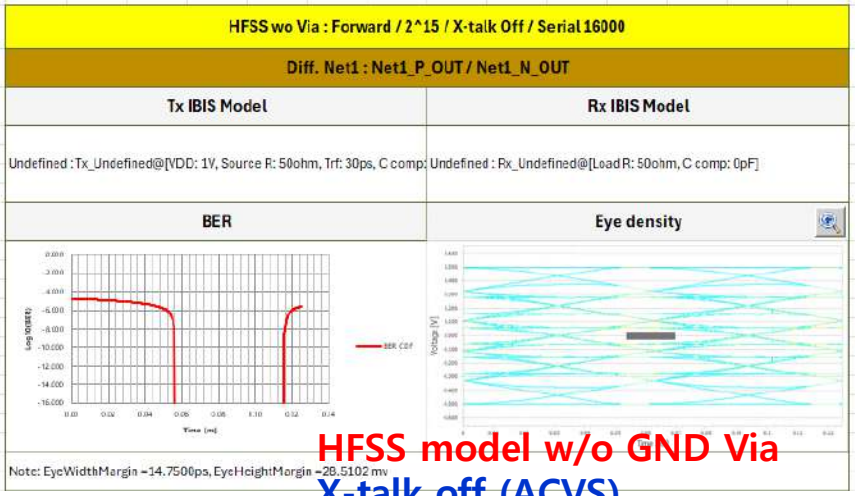
Sig. Via 주변 GND via 에 의한 NEXT/FEXT => HFSS 모델 이용시 Eye/BER 결과



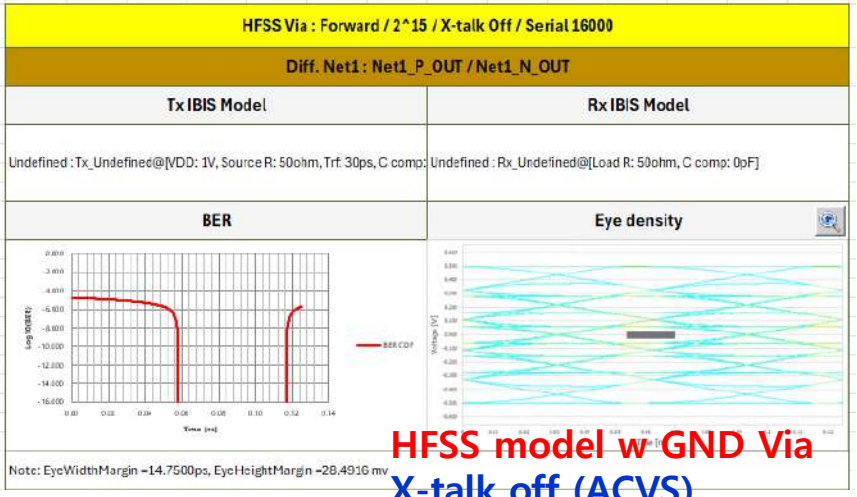
HFSS model w/o GND Via
X-talk on (ACVS)



HFSS model w GND Via
X-talk on (ACVS)



HFSS model w/o GND Via
X-talk off (ACVS)



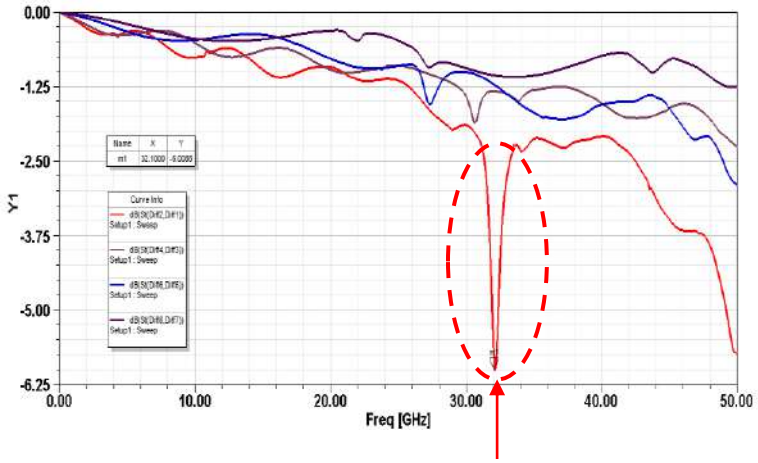
HFSS model w GND Via
X-talk off (ACVS)

2. 시뮬레이션 통한 SI 설계

PCB Resonance Effect :

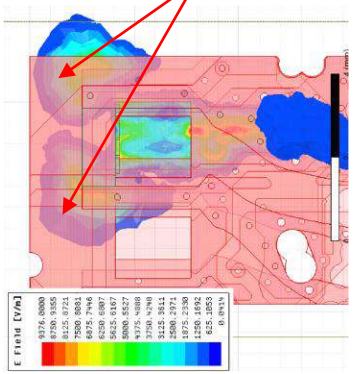
PCB 공진 제거 :

- PCB EM SI/PI : SIwave/HFSS 이용 PCB Ground 의 공진 확인 및 GND via 추가하여 공진 제거

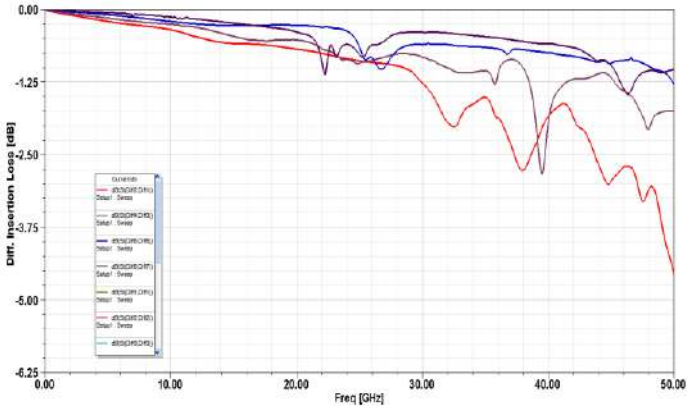


PCB 공진에 의한 SI 문제 확인

공진 위치에 GND via 추가하여 아트웍 수정



SIwave/HFSS 분석 공진 위치 확인 및 수정



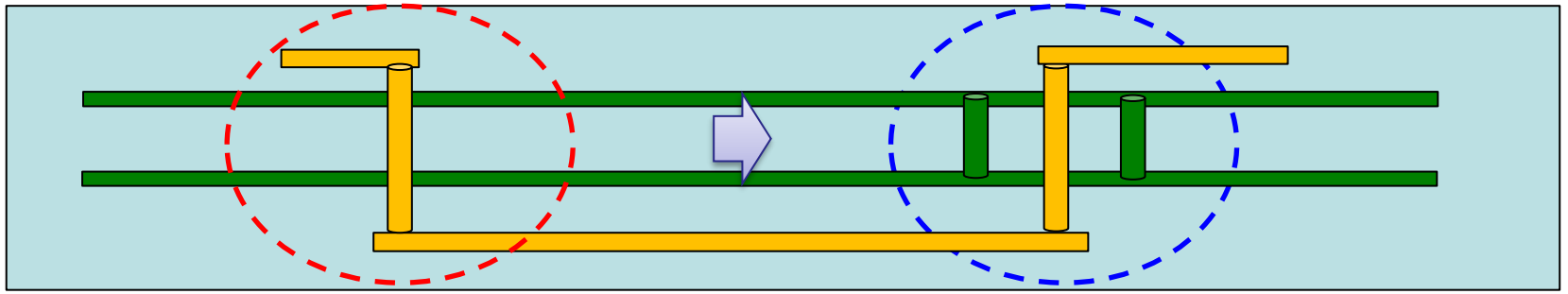
PCB 공진에 의한 SI 문제 해결됨

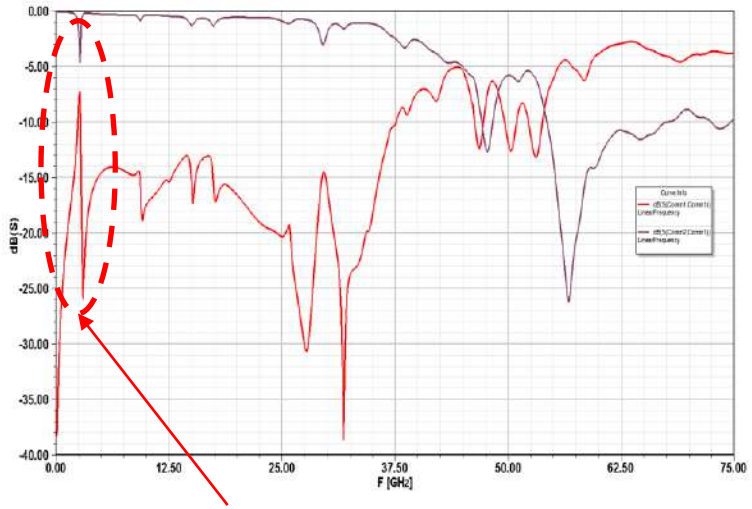
2. 시뮬레이션 통한 SI 설계

PCB Signal Return Resonance Effect :

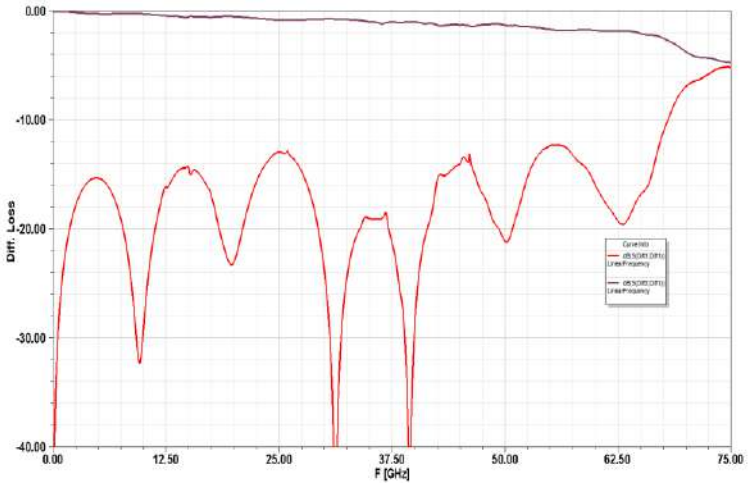
PCB signal return path 문제 해결 :

- PCB EM SI/PI : SIwave 이용 PCB signal 주변 및 층간 연결 via 에 의한 return path 문제 확인하여 cross-talk 및 SI 문제 해결





PCB signal return path 문제 확인



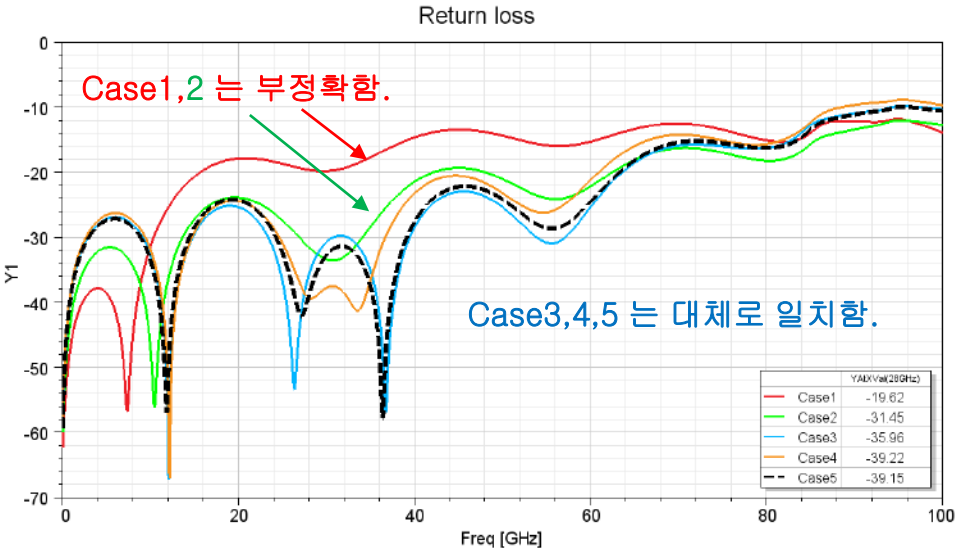
return path 문제 수정 후 결과 개선됨

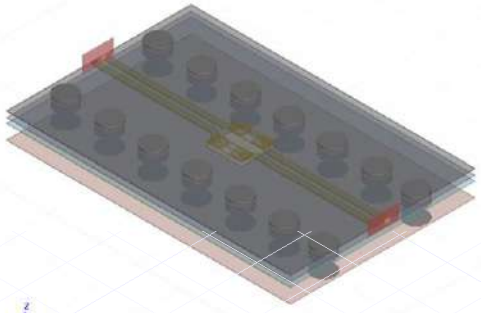
2. 시뮬레이션 통한 SI 설계

AC coupling Capacitor : PSR, 납 형상 영향

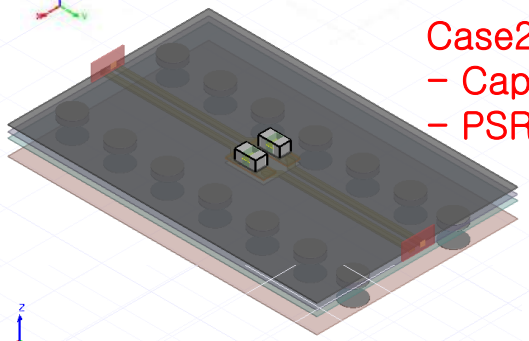
AC coupling Capacitor 모델링에 따른 영향 : RL

- 3D EM : HFSS(High Freq.) 이용 분석 :

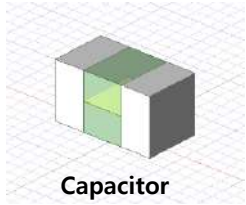


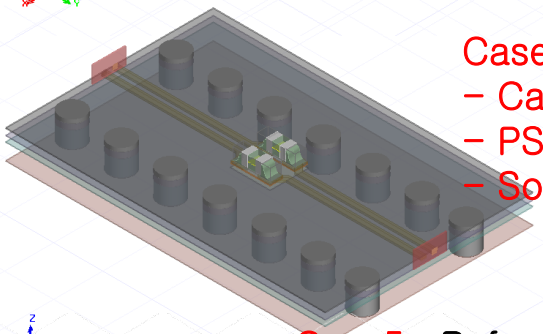


Case1 :
- Ideal C 값 적용
- PSR 레이어 설정

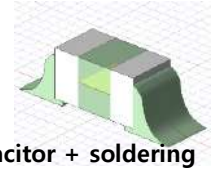


Case2 :
- Capacitor 3D Component 적용
- PSR 레이어 설정

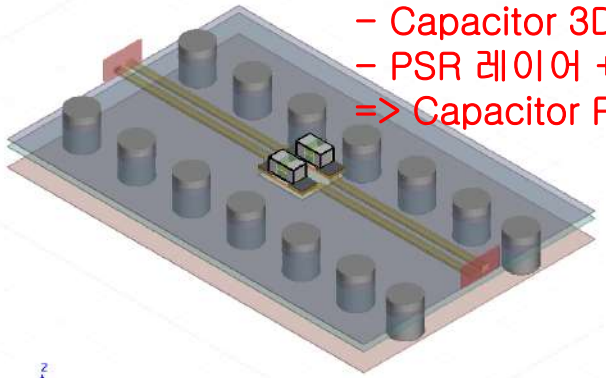


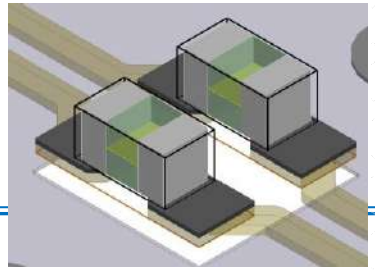


Case3 :
- Capacitor 3D Component 적용
- PSR 레이어 설정
- Solder 형상 적용

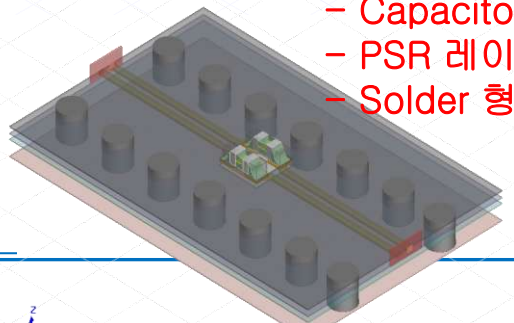


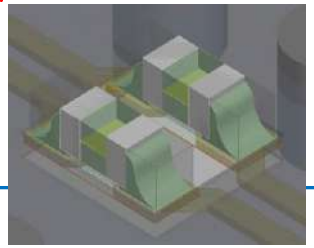
Case4 :
- Capacitor 3D Component 적용
- PSR 레이어 + metal mask 설정
=> Capacitor PAD 부분 metal 채움 PSR 제거





Case5 : Reference 세팅
- Capacitor 3D Component 적용
- PSR 레이어 => Capacitor 부분 PSR 제거
- Solder 형상 적용



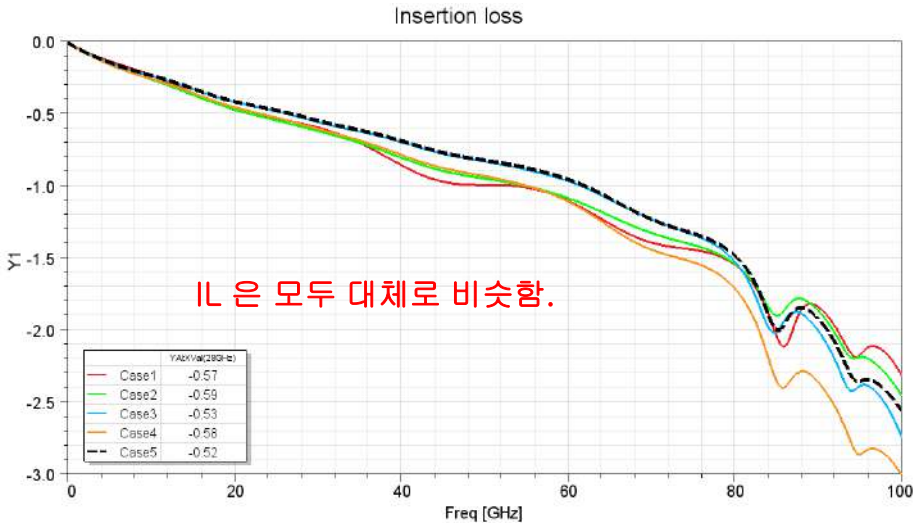


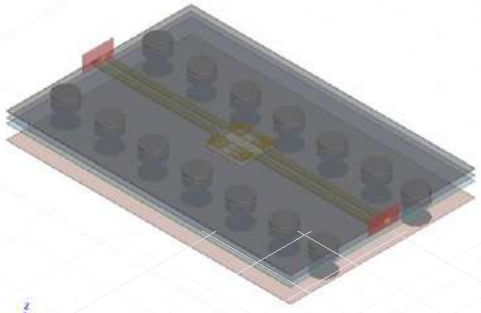
2. 시뮬레이션 통한 SI 설계

AC coupling Capacitor : PSR, 납 형상 영향

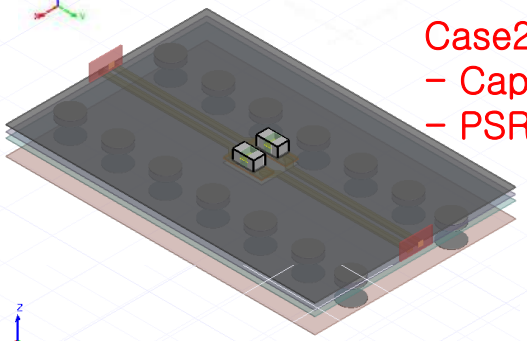
AC coupling Capacitor 모델링에 따른 영향 : IL

- 3D EM : HFSS(High Freq.) 이용 분석 :

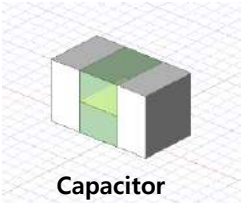




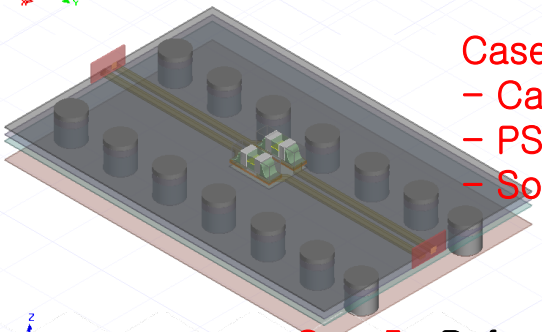
Case1 :
- Ideal C 값 적용
- PSR 레이어 설정



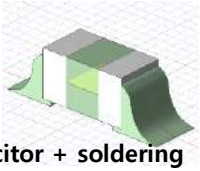
Case2 :
- Capacitor 3D Component 적용
- PSR 레이어 설정



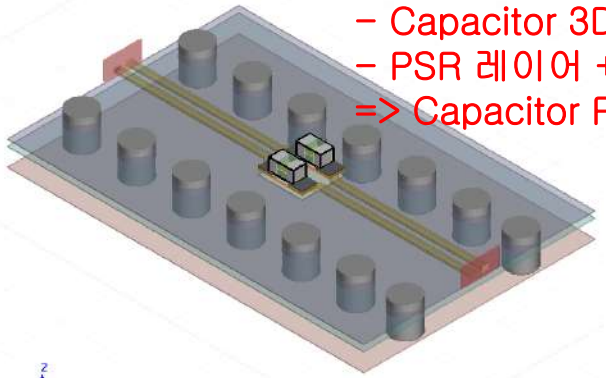
Capacitor
3D component



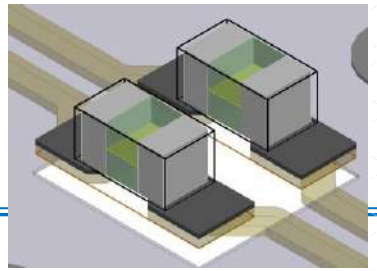
Case3 :
- Capacitor 3D Component 적용
- PSR 레이어 설정
- Solder 형상 적용

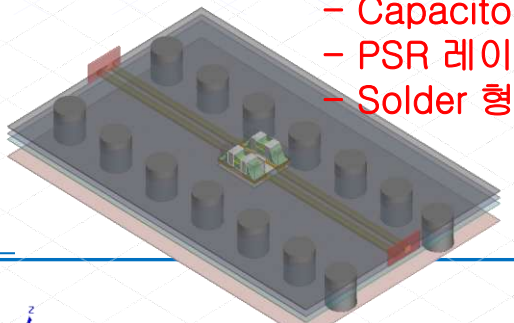


Capacitor + soldering
3D component

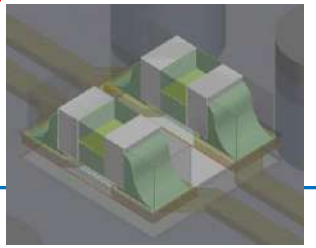


Case4 :
- Capacitor 3D Component 적용
- PSR 레이어 + metal mask 설정
=> Capacitor PAD 부분 metal 채움 PSR 제거





Case5 : Reference 세팅
- Capacitor 3D Component 적용
- PSR 레이어 => Capacitor 부분 PSR 제거
- Solder 형상 적용

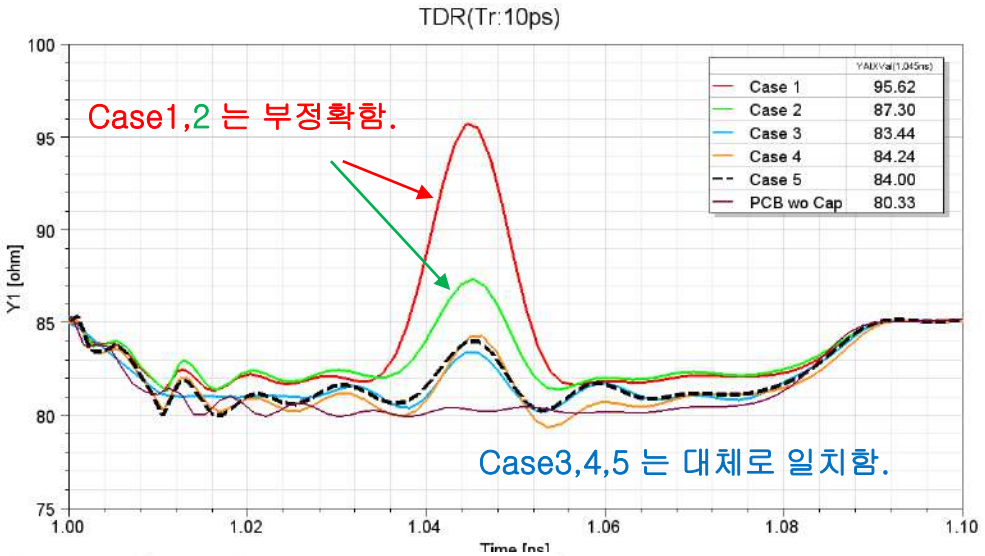


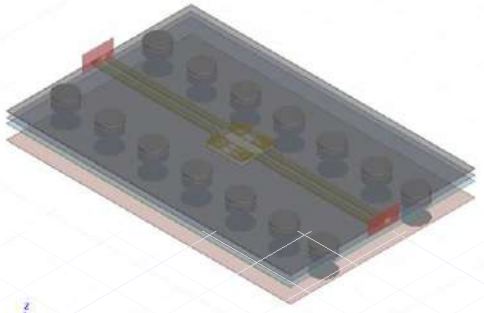
2. 시뮬레이션 통한 SI 설계

AC coupling Capacitor : PSR, 납 형상 영향

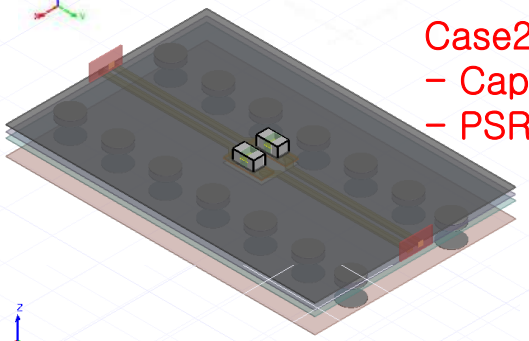
AC coupling Capacitor 모델링에 따른 영향 : TDR

- 3D EM : HFSS(High Freq.) 이용 분석 :

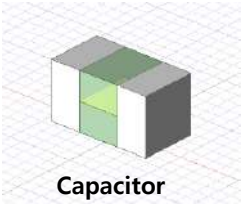


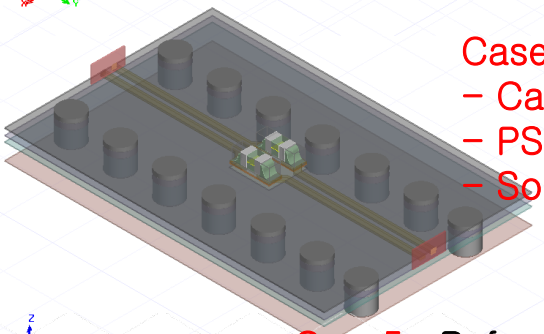


Case1 :
- Ideal C 값 적용
- PSR 레이어 설정

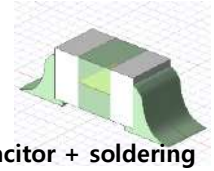


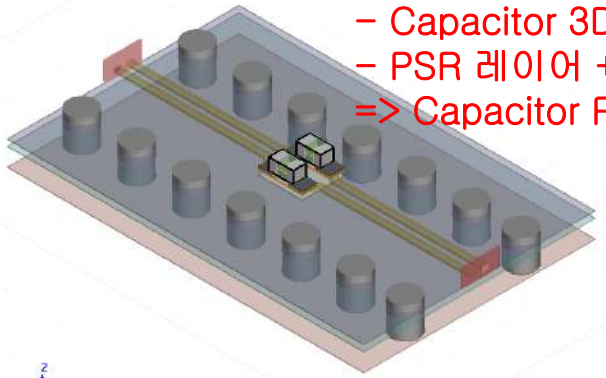
Case2 :
- Capacitor 3D Component 적용
- PSR 레이어 설정



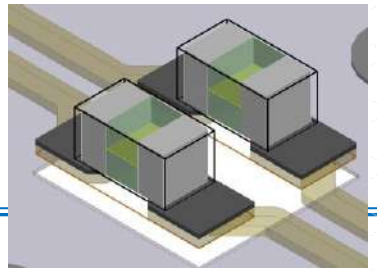


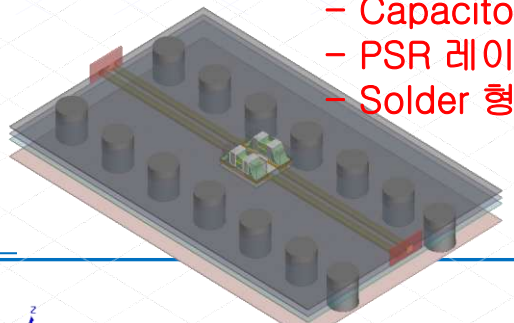
Case3 :
- Capacitor 3D Component 적용
- PSR 레이어 설정
- Solder 형상 적용



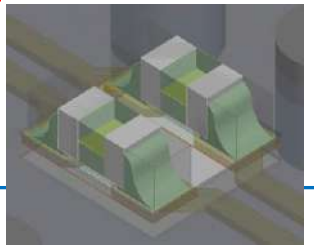


Case4 :
- Capacitor 3D Component 적용
- PSR 레이어 + metal mask 설정
=> Capacitor PAD 부분 metal 채움 PSR 제거



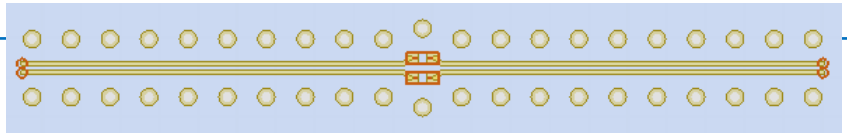


Case5 : Reference 세팅
- Capacitor 3D Component 적용
- PSR 레이어 => Capacitor 부분 PSR 제거
- Solder 형상 적용



2. 시뮬레이션 통한 SI 설계

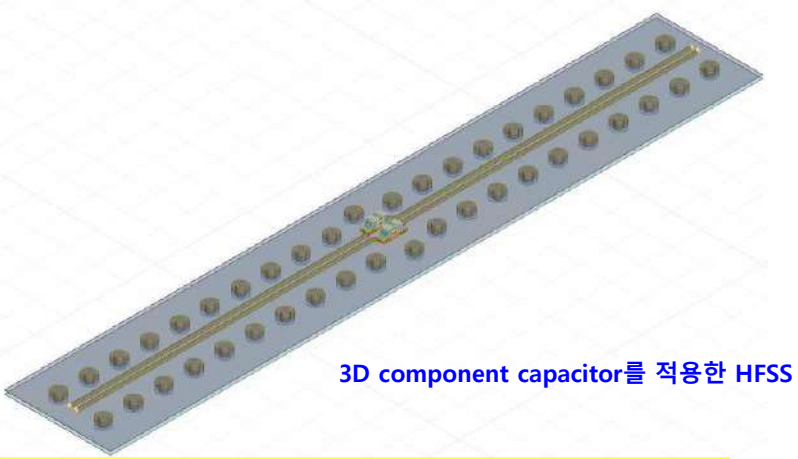
AC coupling Capacitor : SIwave vs. HFSS



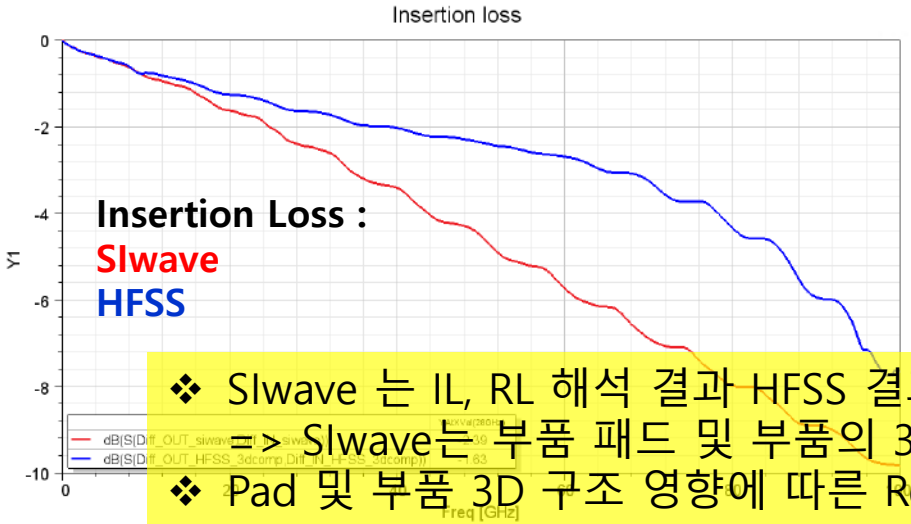
Ideal capacitor를 적용한 SIwave

AC coupling Capacitor 영향 : SIwave vs. HFSS

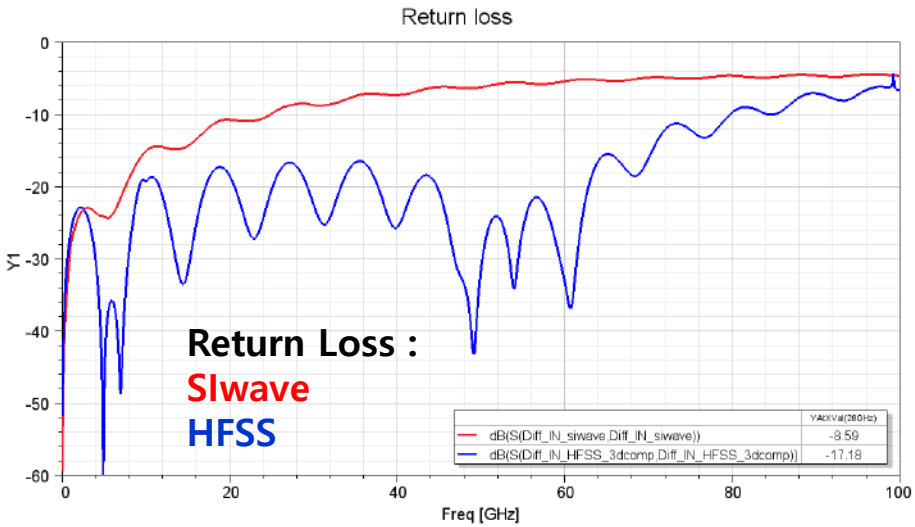
- 3D EM : HFSS(High Freq.) 이용 분석 : 7분 (32cores, 512GB RAM)

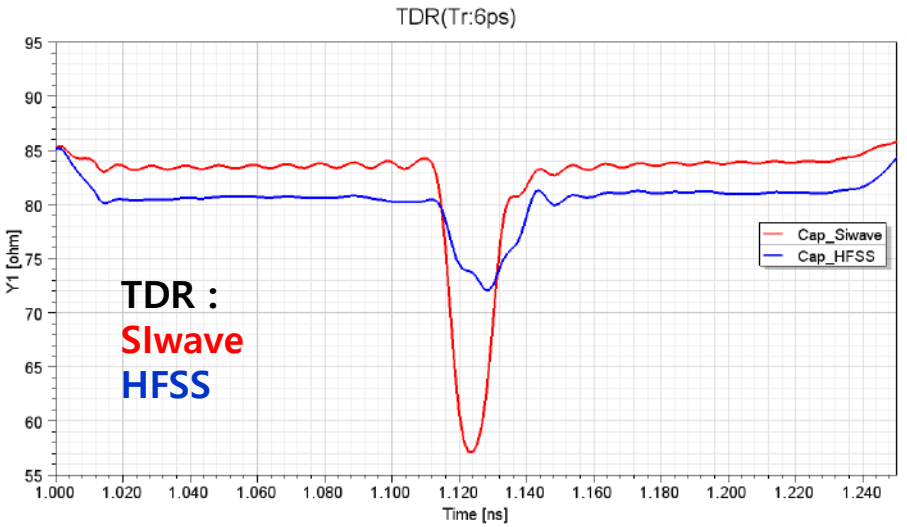


3D component capacitor를 적용한 HFSS



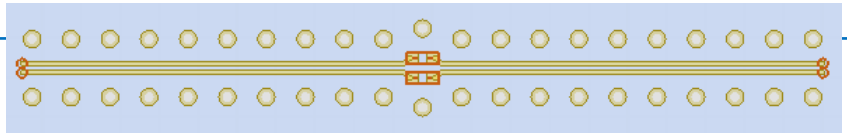
❖ SIwave 는 IL, RL 해석 결과 HFSS 결과 대비 약 10GHz 이상 대역부터 오차가 발생함
=> SIwave는 부품 패드 및 부품의 3D 구조 영향 분석 불가함.
❖ Pad 및 부품 3D 구조 영향에 따른 Ref. plane 최적화를 위해서는 HFSS 분석이 필수임.





2. 시뮬레이션 통한 SI 설계

AC coupling Capacitor : SIwave vs. HFSS

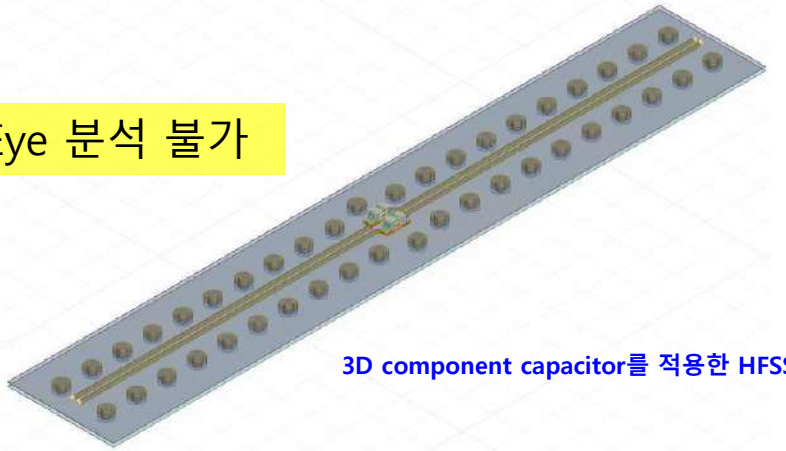


Ideal capacitor를 적용한 SIwave

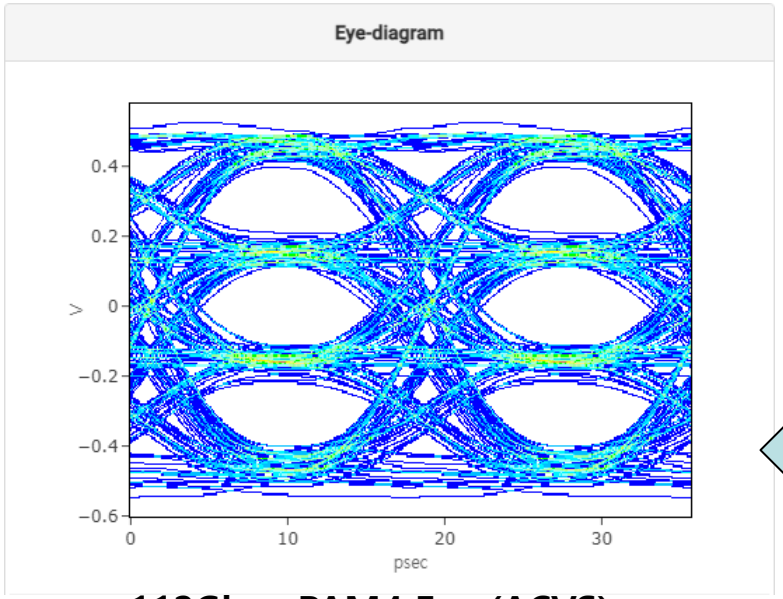
AC coupling Capacitor 영향 : SIwave vs. HFSS

- 3D EM : HFSS(High Freq.) 이용 분석 : 7분 (32cores, 512GB RAM)

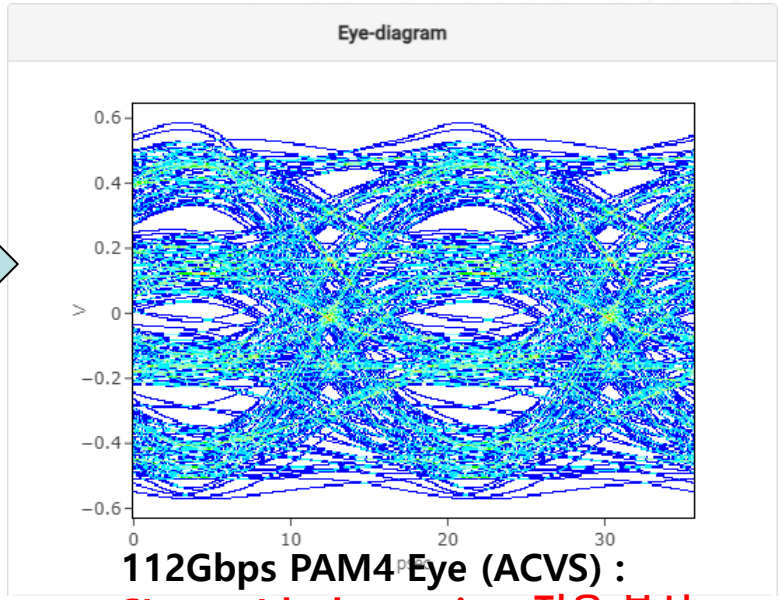
❖ SIwave 의 Ideal Capacitor 이용한 분석으로는 정확한 Eye 분석 불가



3D component capacitor를 적용한 HFSS



112Gbps PAM4 Eye (ACVS) :
HFSS 3D Component capacitor 적용 Ref. plane 최적화 분석



112Gbps PAM4 Eye (ACVS) :
SIwave Ideal capacitor 적용 분석
=> Ref. plane 최적화 불가

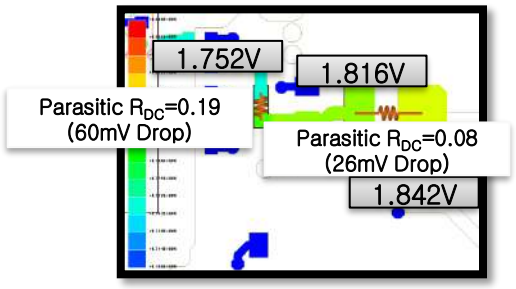
2. 시뮬레이션 통한 SI 설계

분석 및 설계 최적화 방법 :

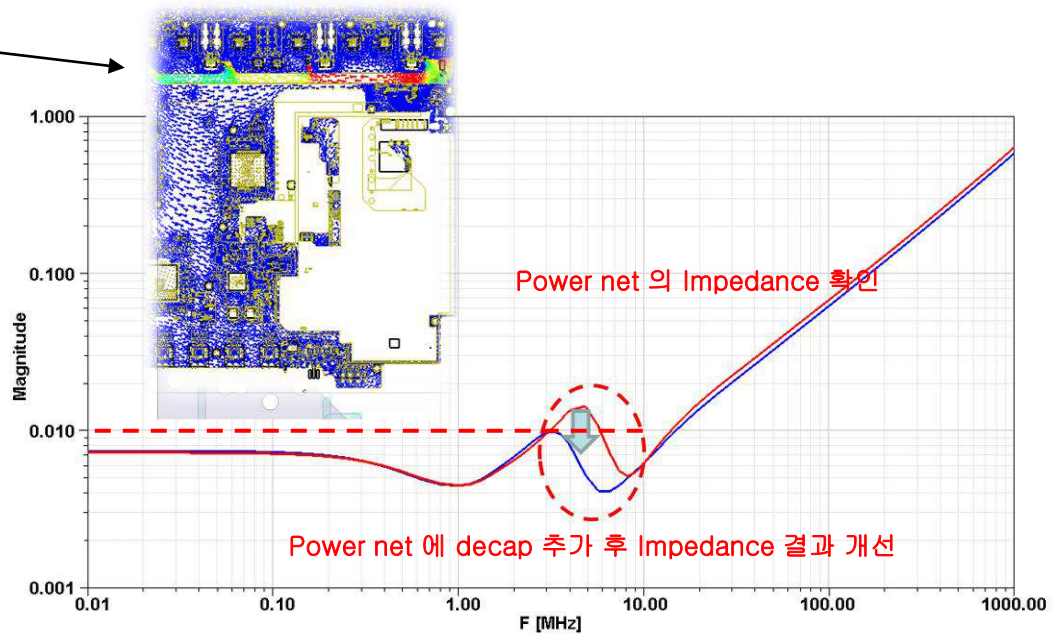
PCB Power Ground PI 분석 및 최적화 :

- PCB EM SI/PI : SIwave 이용 Power Net 의 IR Drop (전압 분포), 전류 분포 및 Impedance 분석 후 결과 개선 필요.
- Powe Net 의 Impedance 개선으로 Power noise 에 의한 문제 개선함.

Power net 의 전압 분포, IR Drop 확인



Power net 의 전압 분포, IR Drop 확인

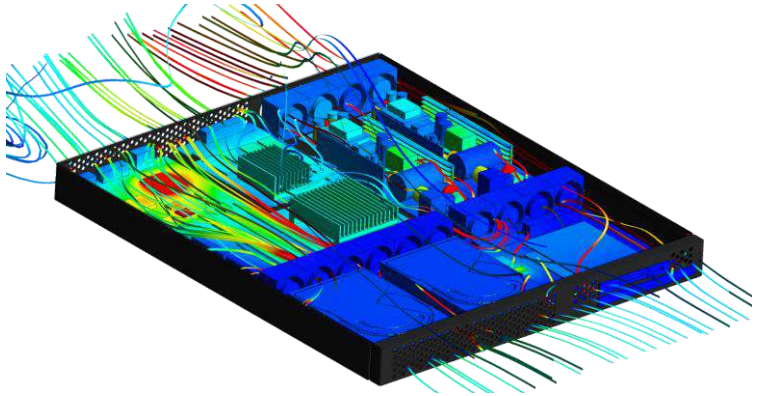


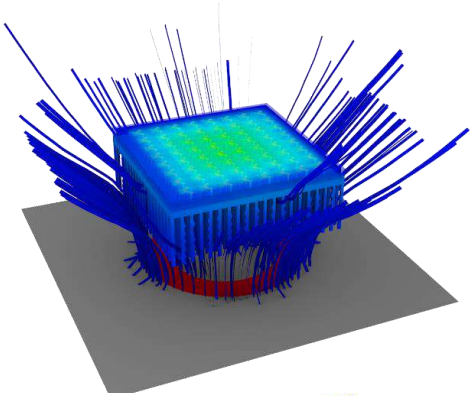
2. 시뮬레이션 통한 SI 설계

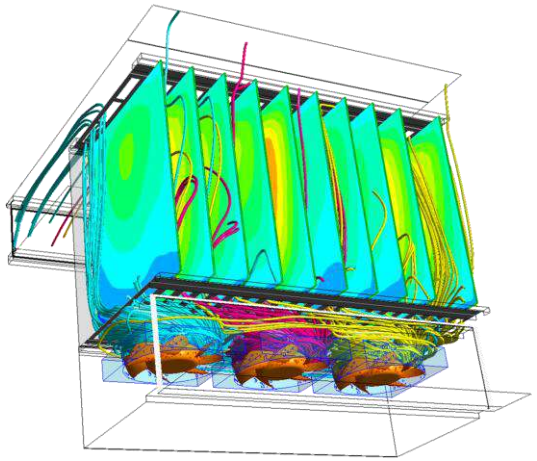
분석 및 설계 최적화 방법 :

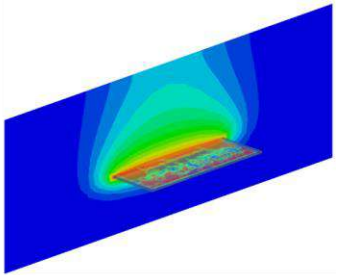
Icepak :

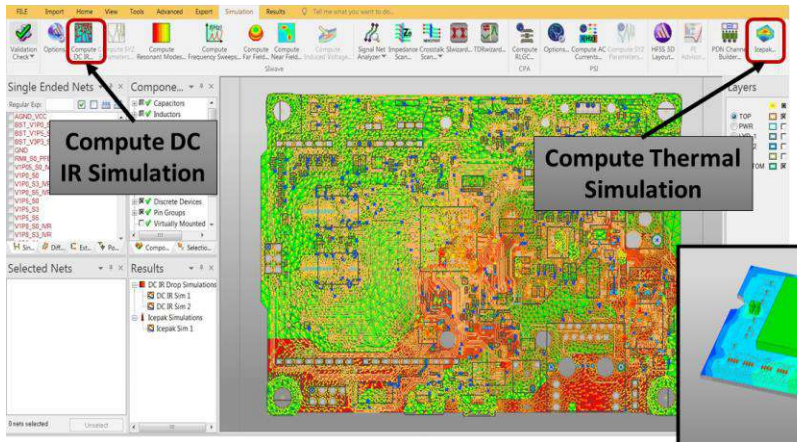
- Electronics thermal management
- Airflow, temperature, heat transfer in IC packages, PCBs, electronic assemblies, power electronics

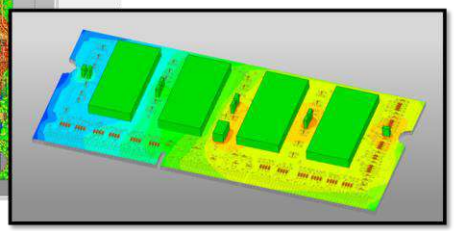


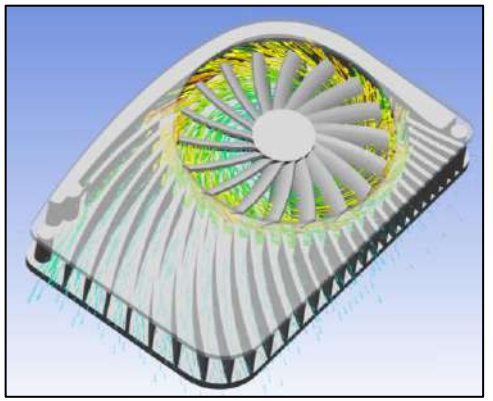










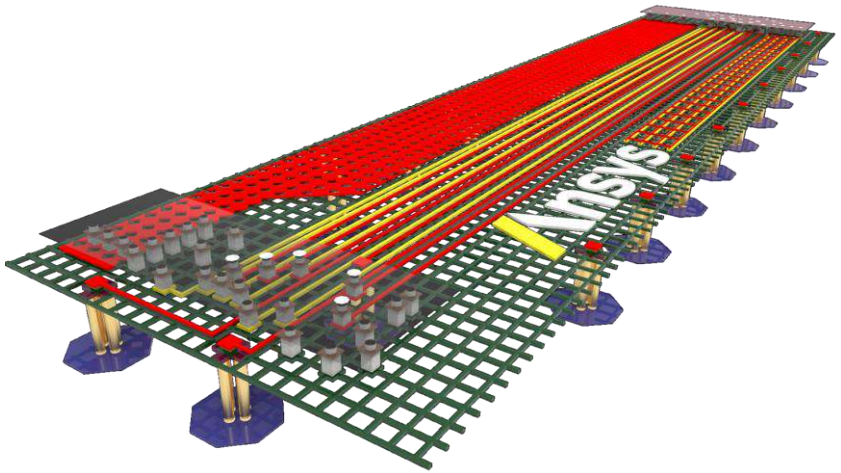


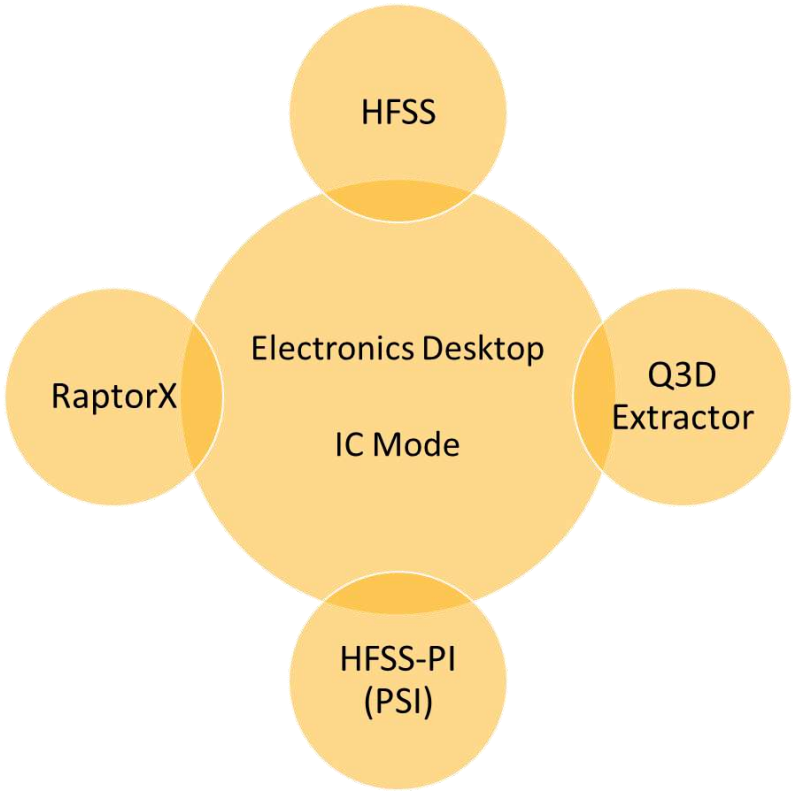
2. 시뮬레이션 통한 SI 설계

분석 및 설계 최적화 방법 :

Electronics Enterprise : 3D Layout Design Mode for IC workflow

- IC/Semiconductor Applications
  - IC Components
  - Interposers – SI/PI
  - IC Bus
  - System – IC/Package





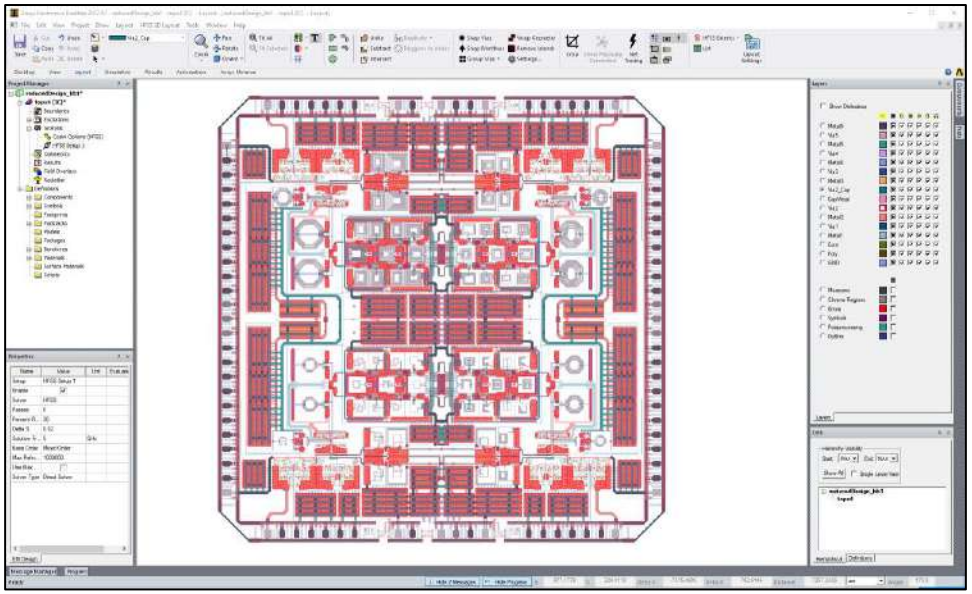
분석 및 설계 최적화 방법 :

Electronics Enterprise : 3D Layout Design Mode for IC workflow

A specialized 3D Layout Design Mode for the IC Workflow

2023 R2

- System assembly
  - IC-mode on General
  - Select physically connected with IC-mode on General
- Point-based Terminal Port
- Pin Group dialog
- Arc reconstruction
- Speed optimizations
- New GDS exporter
- Enhanced GDS import logging and progress bar



2. 시뮬레이션 통한 SI 설계

분석 및 설계 최적화 방법 :

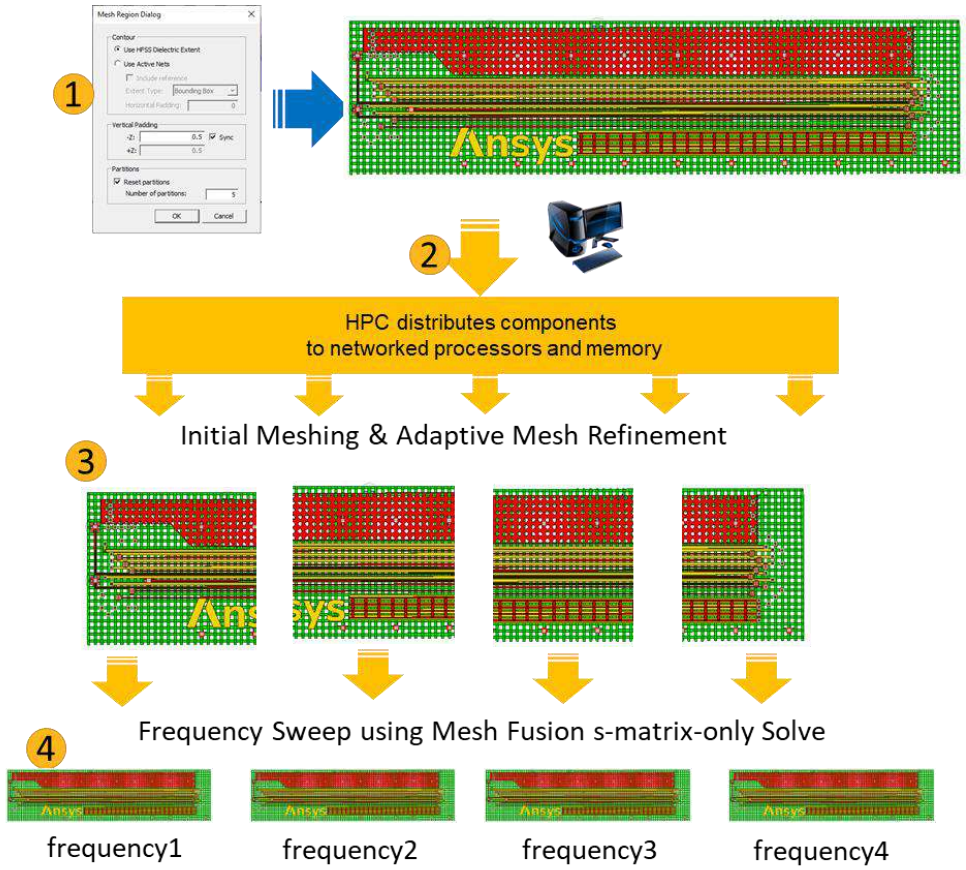
Electronics Enterprise : 3D Layout Design Mode for IC workflow

HFSS Parallel Adaptive Refinement in 3DL IC mode

- Parallel adaptive mesh process
  1. Automatic partitioning for adaptive refinement
  2. Refine domains independently
  3. Evaluate fully coupled system using Mesh Fusion
- Simplified initial meshing
- Extra level of distribution during adaptive refinement
- No compromise for frequency sweep

Auto 48 cores	Initial Mesh	Adaptive Meshing		Interpolating Sweep	
		Time	Mem (GB)	Time	Mem (GB)
Conformal	01:16:29	14:12:05	822	52:47:04	844/894
Component Adapt	00:22:46	02:55:55	142	05:57:00	113/128

~7.5x



3. Multi-Die PDN 해석을 위한 PEEC 소개

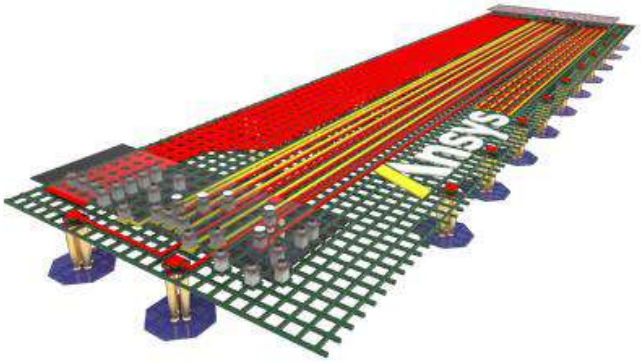
ANSYS Helic RaptorX solver : Fast PDN PEEC extraction solution

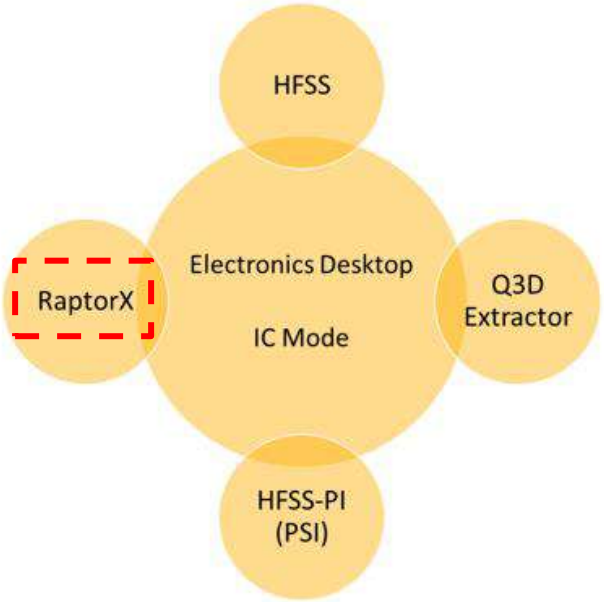
PDN GDS file ⇨ Linux, ANSYS Helic UI => RaptorX

⇨ Windows, ANSYS Electronics UI => RaptorX

Electronics Enterprise : 3D Layout Design Mode for IC workflow

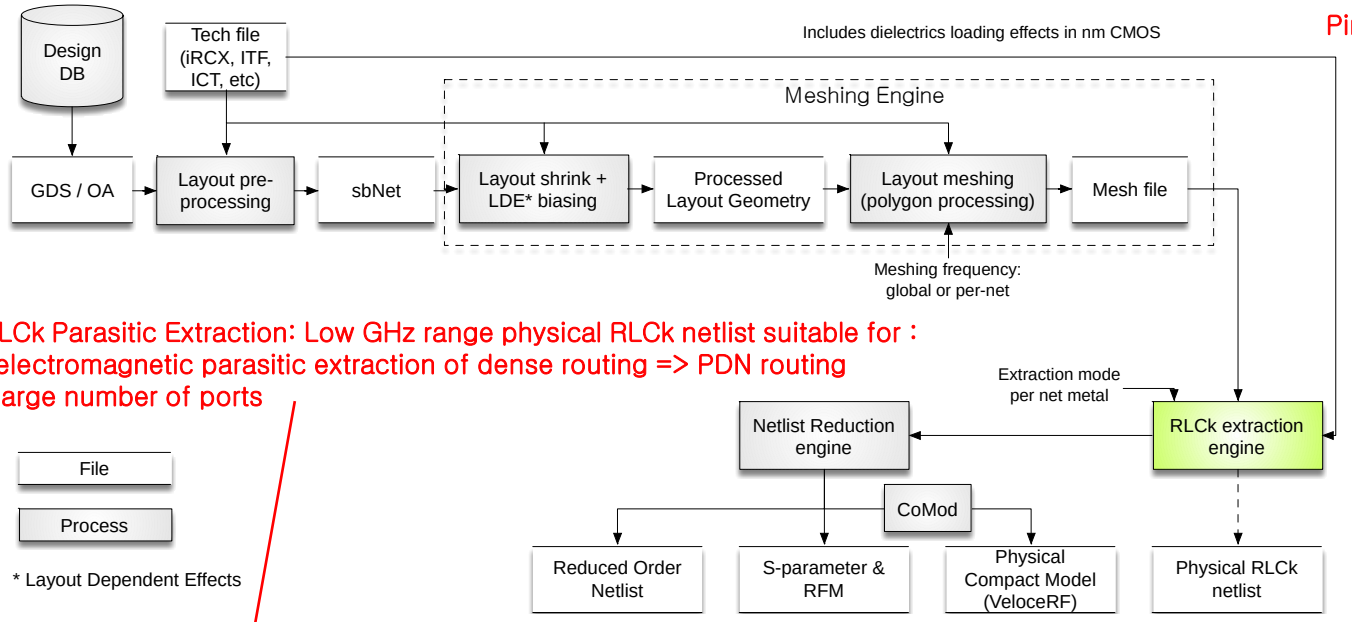
- IC/Semiconductor Applications
  - IC Components
  - Interposers – SI/PI
  - IC Bus
  - System – IC/Package



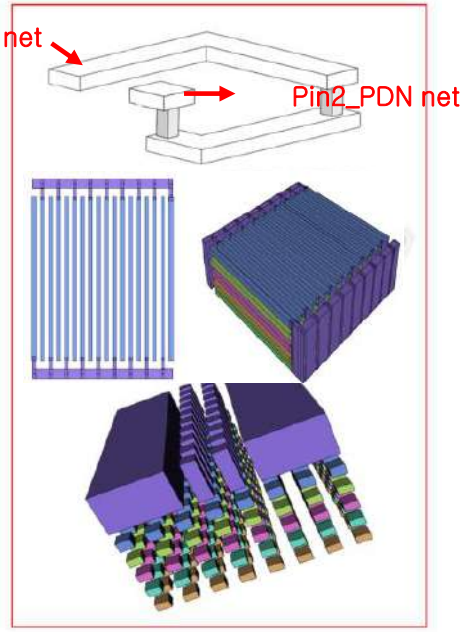


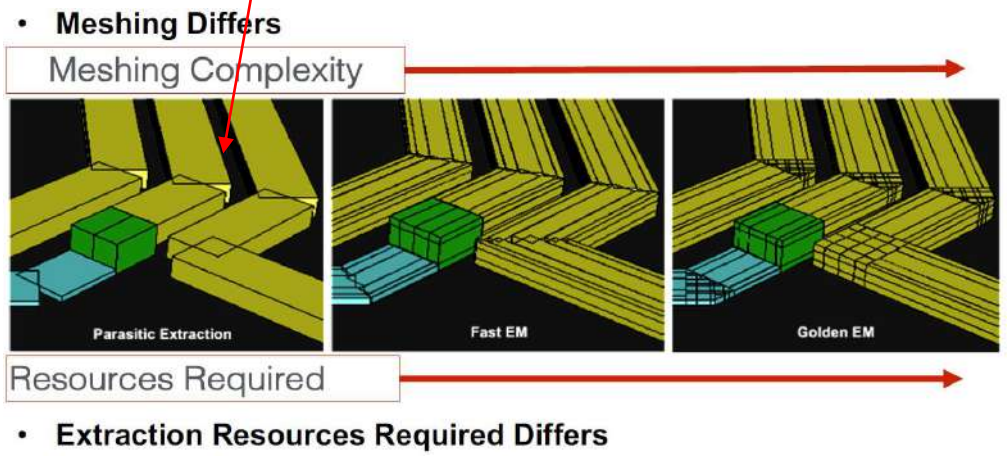
3. Multi-Die PDN 해석을 위한 PEEC 소개

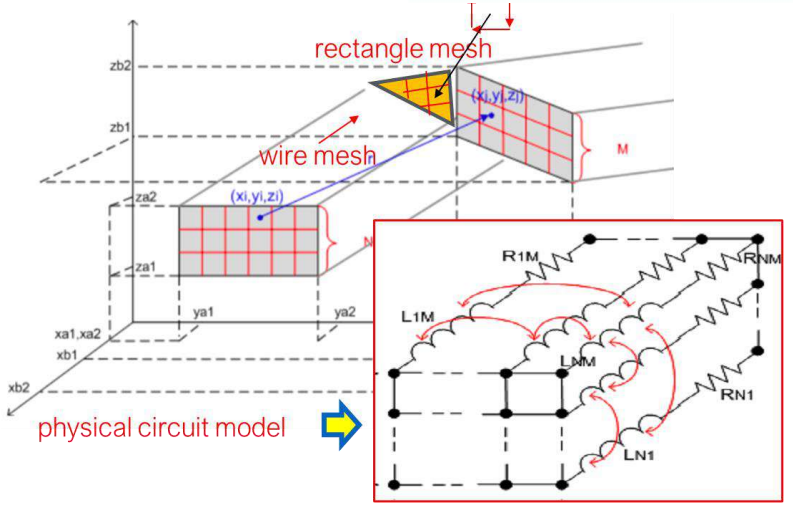
ANSYS Helic RaptorX solver : Fast PDN PEEC extraction solution



- RLCk Parasitic Extraction: Low GHz range physical RLCk netlist suitable for :
  - electromagnetic parasitic extraction of dense routing => PDN routing
  - large number of ports



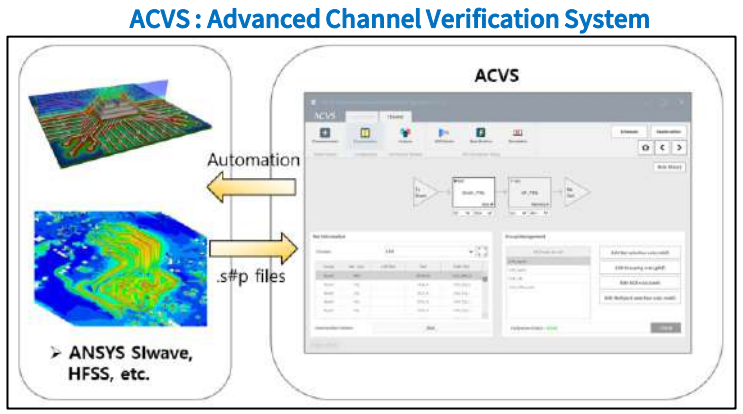




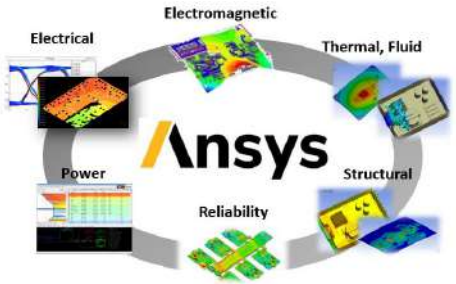
2. 시뮬레이션 통한 SI 설계

Huwin 소개 : 주요 분야

초고속 SI 채널 자동분석 솔루션 (ACVS) 개발 공급



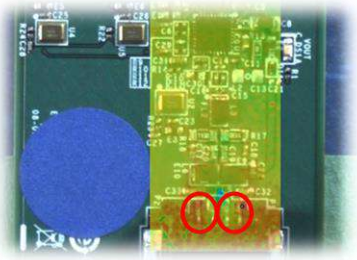
ANSYS Electronics , EMCoS Simulation 툴 공급



SI/PI 컨설팅, Training

고속 채널 SI/PI 측정 및 컨설팅

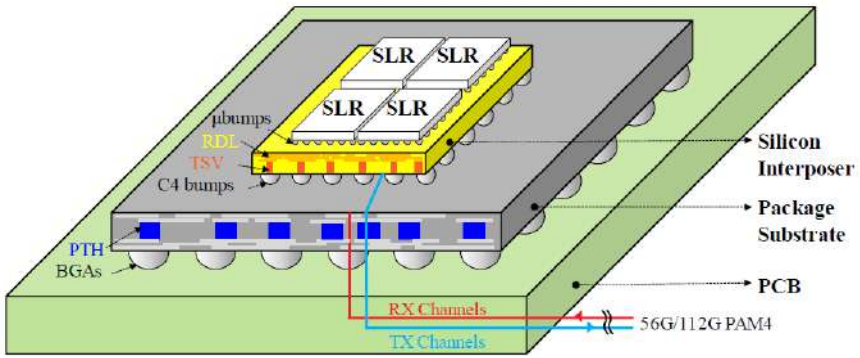
EMC Scan 측정 장비 공급 및 컨설팅



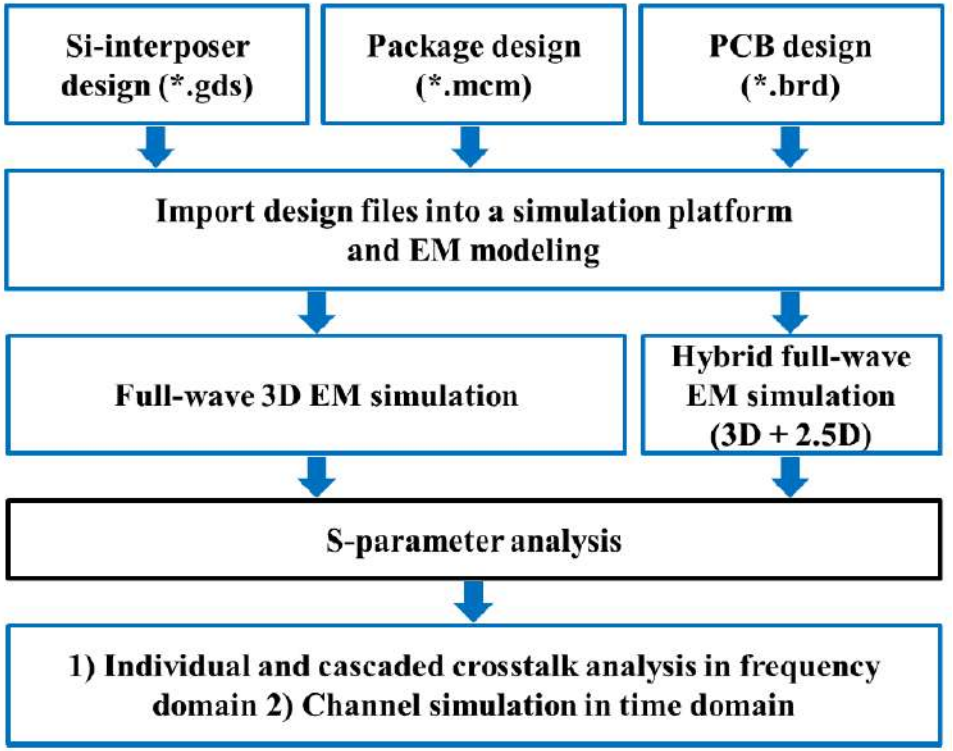
2. DesignCon 2024 자료 소개 자료 소개

2-1 : Crosstalk Noise Optimization For Robust 112G PAM4 Design in Stacked Silicon Interconnect Technology , Leon Chen (AMD Inc) 외

Intro :
- high-density, high bandwidth, low power consumption => 2.5D IC w adv. Pkg tech
- crowded signal and power, tight timing and voltage margin => NEXT/FEXT noises and optimized design
- efficient simulation and verification



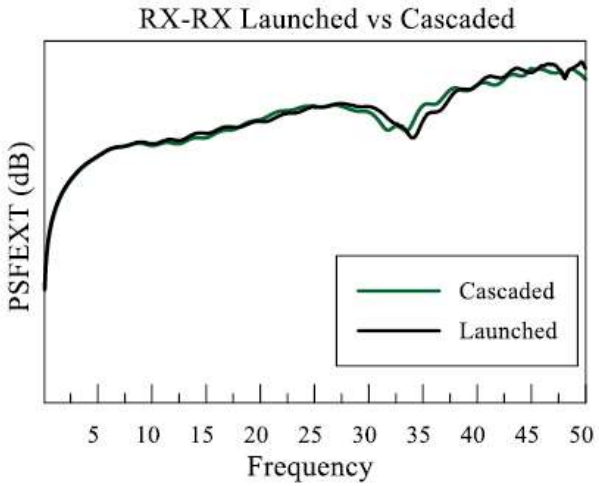
> Adopt a hybrid simulation (3D + 2.5D) method for PCB to save simulation time
> Evaluate the SerDes TX and RX channel's crosstalk at both 14 and 28 GHz which is Nyquist frequency for 56 and 112 Gbps PAM4

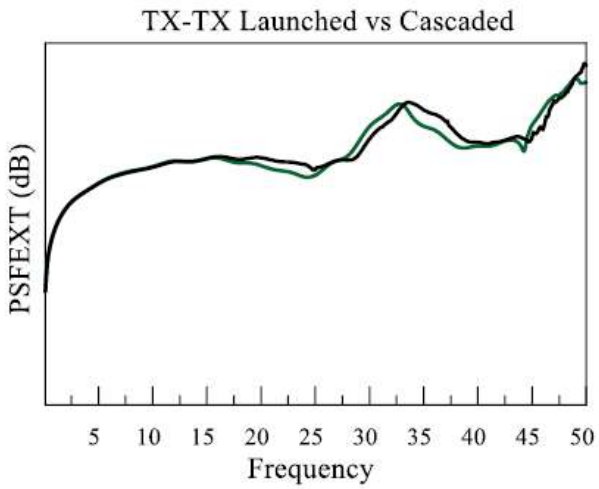


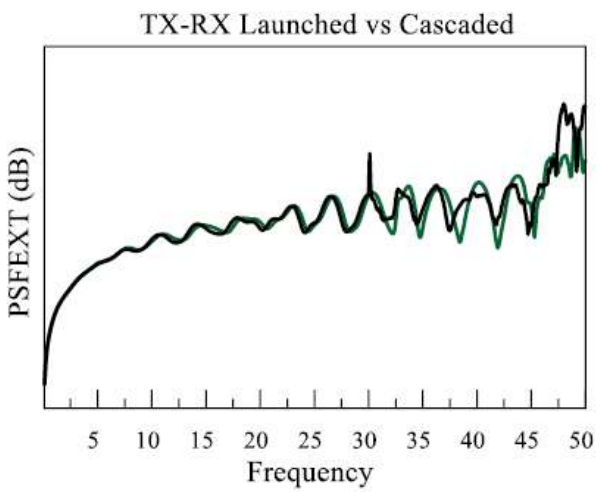
2. DesignCon 2024 자료 소개 자료 소개

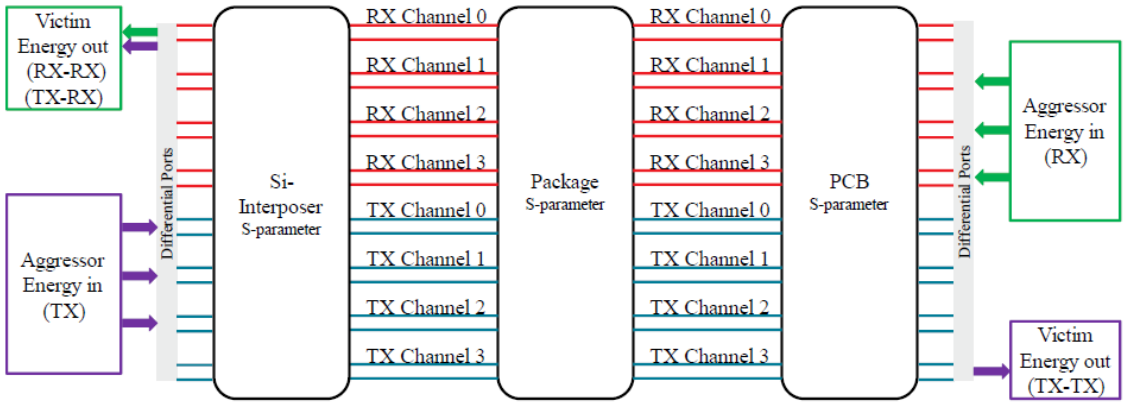
2-1 : Crosstalk Noise Optimization For Robust 112G PAM4 Design in Stacked Silicon Interconnect Technology , Leon Chen (AMD Inc) 외

Launched vs. Cascaded Methodology :
- 80% simulation time saving, 2.1% delta PSFEXT, 0% delta PSNEXT







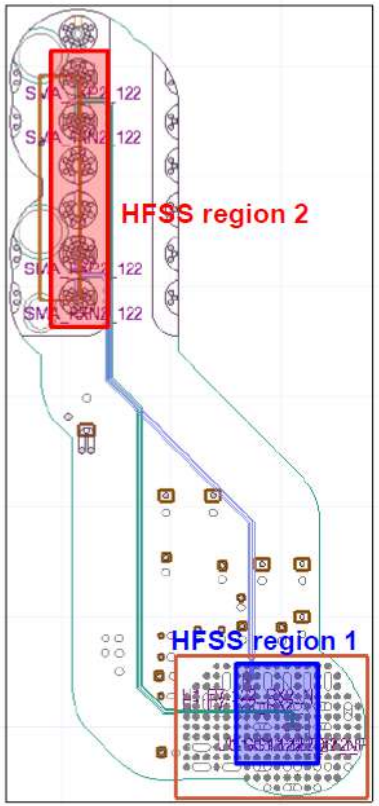


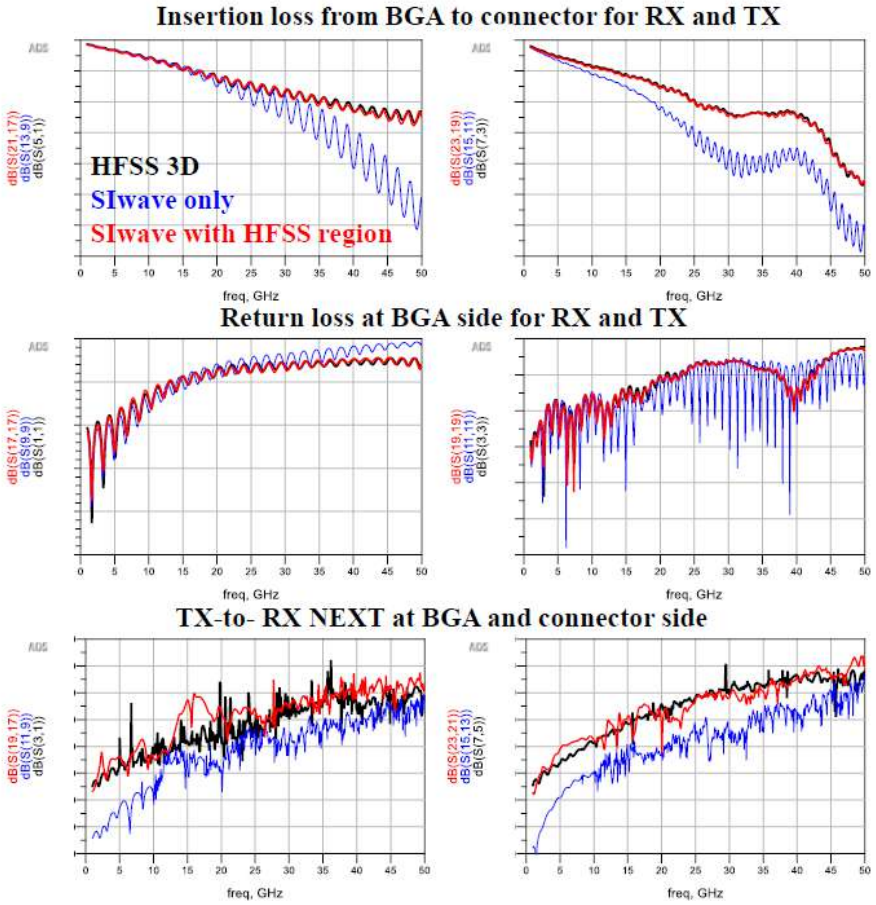
2. DesignCon 2024 자료 소개 자료 소개

2-1 : Crosstalk Noise Optimization For Robust 112G PAM4 Design in Stacked Silicon Interconnect Technology , Leon Chen (AMD Inc) 외

Hybrid Full Wave EM Simulation :

- **Hybrid simulation**
  - 3D: Vertical part (e.g., vias)
  - 2.5D: Horizontal parts (e.g., traces)
- **Comparison**
  - 84% runtime reduction
    - *SIwave with HFSS region (7.2 hrs) ↔ HFSS 3D (45 hrs)*
  - Correlation factor
    - *Insertion loss: > 0.99*
    - *Return loss: > 0.92*
    - *Crosstalk: > 0.86*
- **Limitation of 2.5D-only approach**
  - SIwave-only has a large difference in IL/RL/crosstalk compared to HFSS 3D



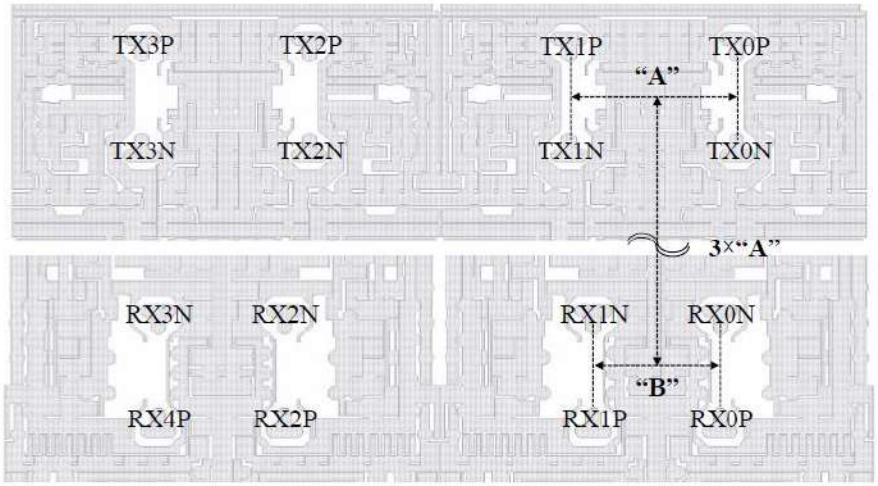


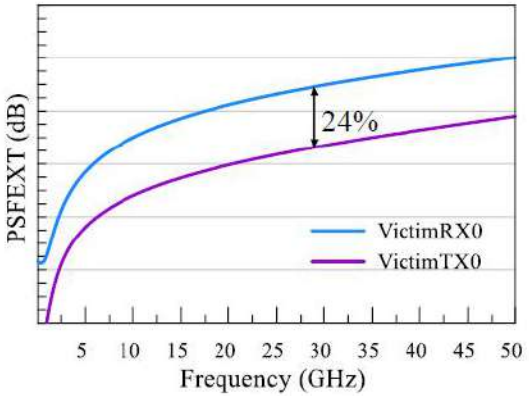
2. DesignCon 2024 자료 소개 자료 소개

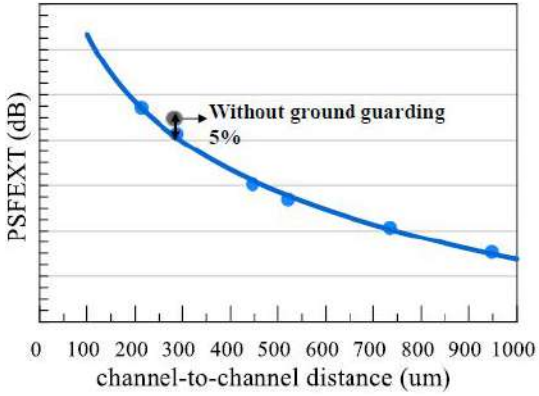
2-1 : Crosstalk Noise Optimization For Robust 112G PAM4 Design in Stacked Silicon Interconnect Technology , Leon Chen (AMD Inc) 외

Crosstalk Optimization : Si Interposer

- **TX's minimum channel-to-channel distance is larger than RX's**
  - PSFEXT TX-TX when TX0 is the victim shows a 24% lower crosstalk level than PSFEXT RX-RX when RX0 is the victim
  - With increasing the channel-to-channel distance, PSFEXT is gradually improved
- **Without a ground guarding, it could affect ~5% penalty in the PSFEXT**





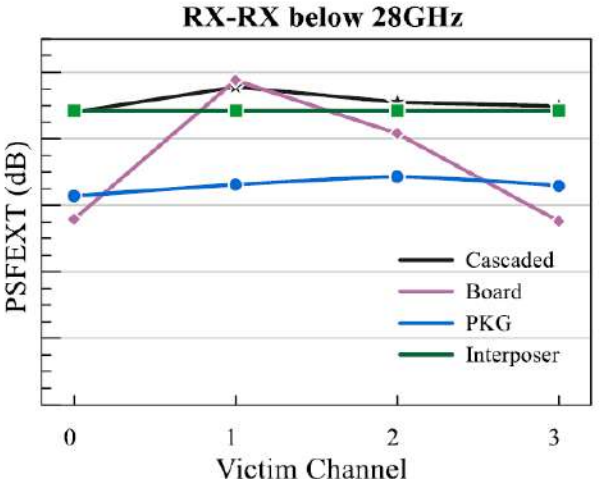


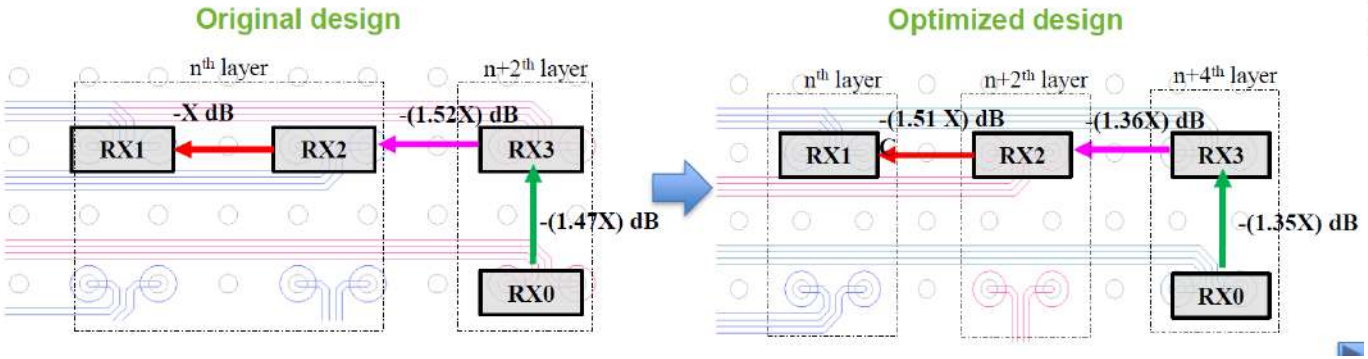
2. DesignCon 2024 자료 소개 자료 소개

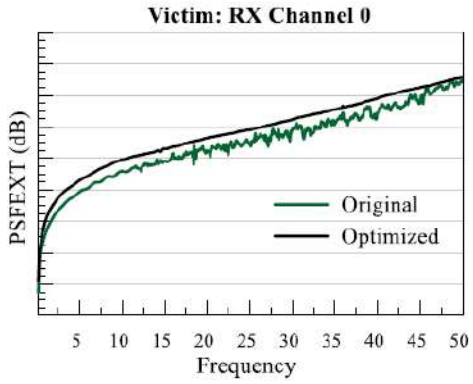
2-1 : Crosstalk Noise Optimization For Robust 112G PAM4 Design in Stacked Silicon Interconnect Technology , Leon Chen (AMD Inc) 외

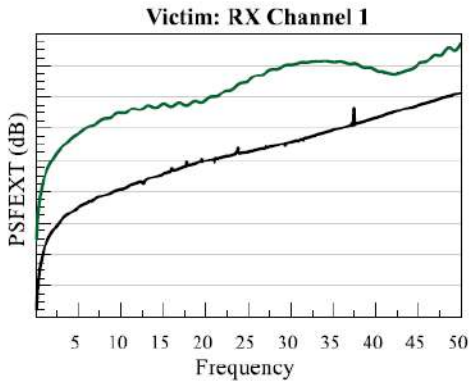
Crosstalk Optimization : PCB

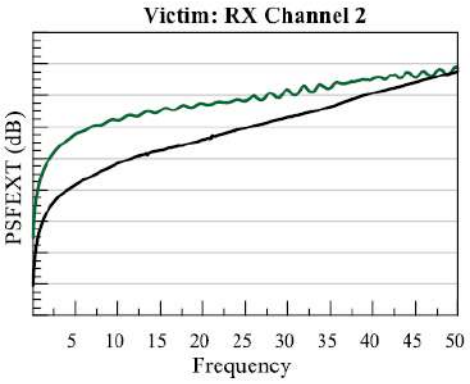
- The channel 1 and 2 are on the n^{th} layer and arranged in the different column of BGA map.
- As the channel 2 traces pass the vertical via of channel 1, EM fields can couple to the vertical vias through the dielectric layer
- Changed RX trace routing layers from *(n^{th} and $n+2^{th}$)* to *(n^{th}, $n+2^{th}$, and $n+4^{th}$)*

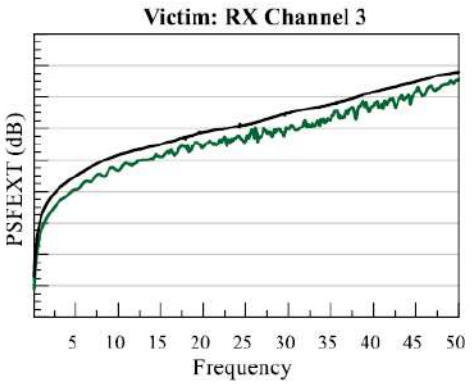










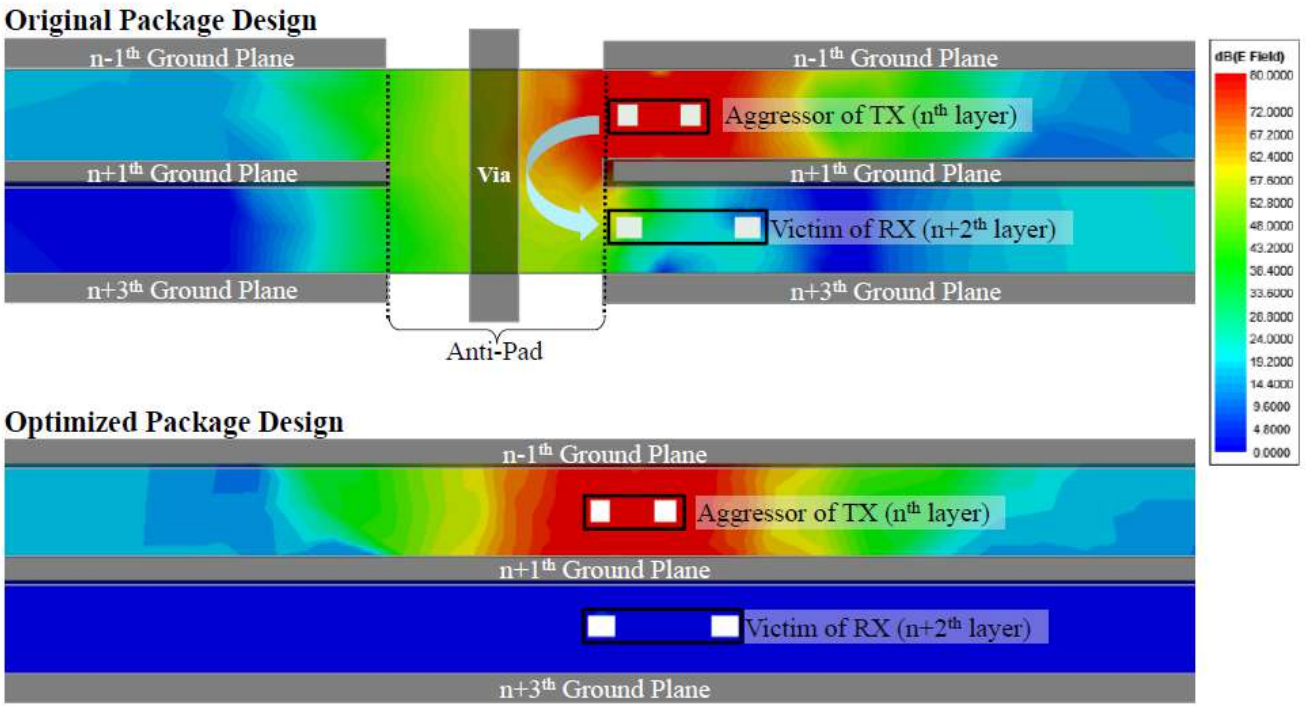


2. DesignCon 2024 자료 소개 자료 소개

2-1 : Crosstalk Noise Optimization For Robust 112G PAM4 Design in Stacked Silicon Interconnect Technology , Leon Chen (AMD Inc) 외

Crosstalk Optimization : PKG

- TX and RX traces are formed on the n^{th} and $n+2^{th}$ layers as a stripline
- Solid ground planes are placed on the $n-1^{th}$, $n+1^{th}$, and $n+3^{th}$ layers
- The via's anti-pad can create an inevitable path for energy to pass through

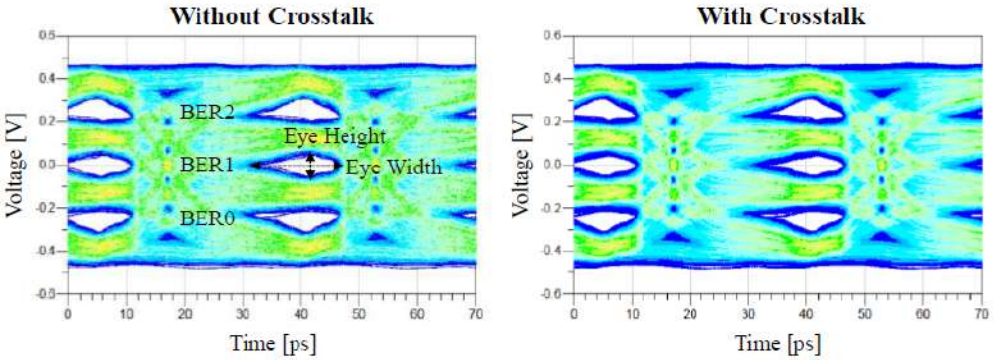


2. DesignCon 2024 자료 소개

2-1 : Crosstalk Noise Optimization For Robust 112G PAM4 Design in Stacked Silicon Interconnect Technology , Leon Chen (AMD Inc) 외

Crosstalk Optimization : Entire Channel Simulation in Time Domain

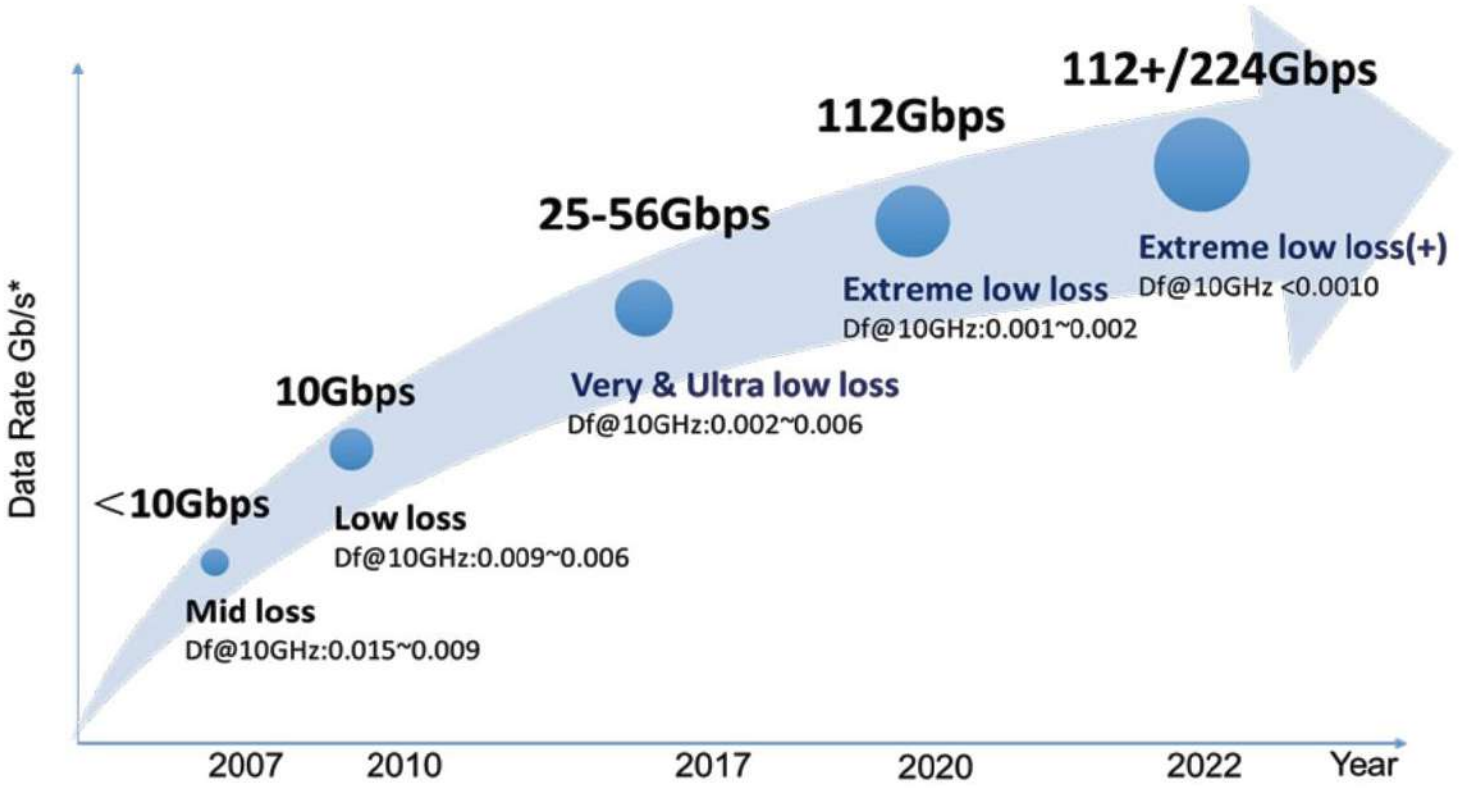
- **Time domain simulation**
  - 112G PAM4 signal with 500mV$_{pp}$ is generated by TX AMI model
  - Transmitted PAM4 signal to RX AMI model through the Si interposer, package, and PCB S-parameter models
- **Cascaded result of PSFEXT RX-RX**
  - Crosstalk noise affects 6.6% eye height and 5.2% eye width degradation
- **Cascaded result of PSNEXT TX-RX**
  - No influence on the optimized design
  - Very low crosstalk effect in the time domain



Delta between w/ and w/o crosstalk noise	FEXT RX-RX		NEXT TX-RX	
	Original design	Optimized design	Original design	Optimized design
Eye Height at BER0 [%]	-6.2	0.0	0.0	0.0
Eye Height at BER1 [%]	-8.0	0.0	0.0	-1.3
Eye Height at BER2 [%]	-5.8	0.0	0.0	-1.0
Average [%]	**6.6**	**0.0**	**0.0**	**0.7**
Eye Width at BER0 [%]	-6.6	0.0	0.0	0.0
Eye Width at BER1 [%]	-3.8	0.0	0.0	0.0
Eye Width at BER2 [%]	-5.2	0.0	0.0	-1.5
Average [%]	**5.2**	**0.0**	**0.0**	**0.5**

2-2 : 224G Ultra-low Loss PCB Solution , Scarlet Wang (Shengyi Technology) 외

PCB High-Speed Material Evolution Acceleration :



224G PCB Material Dielectric Target

Loss Improvement

20-30%

Dielectric Df

< 0.0006

@10GHz

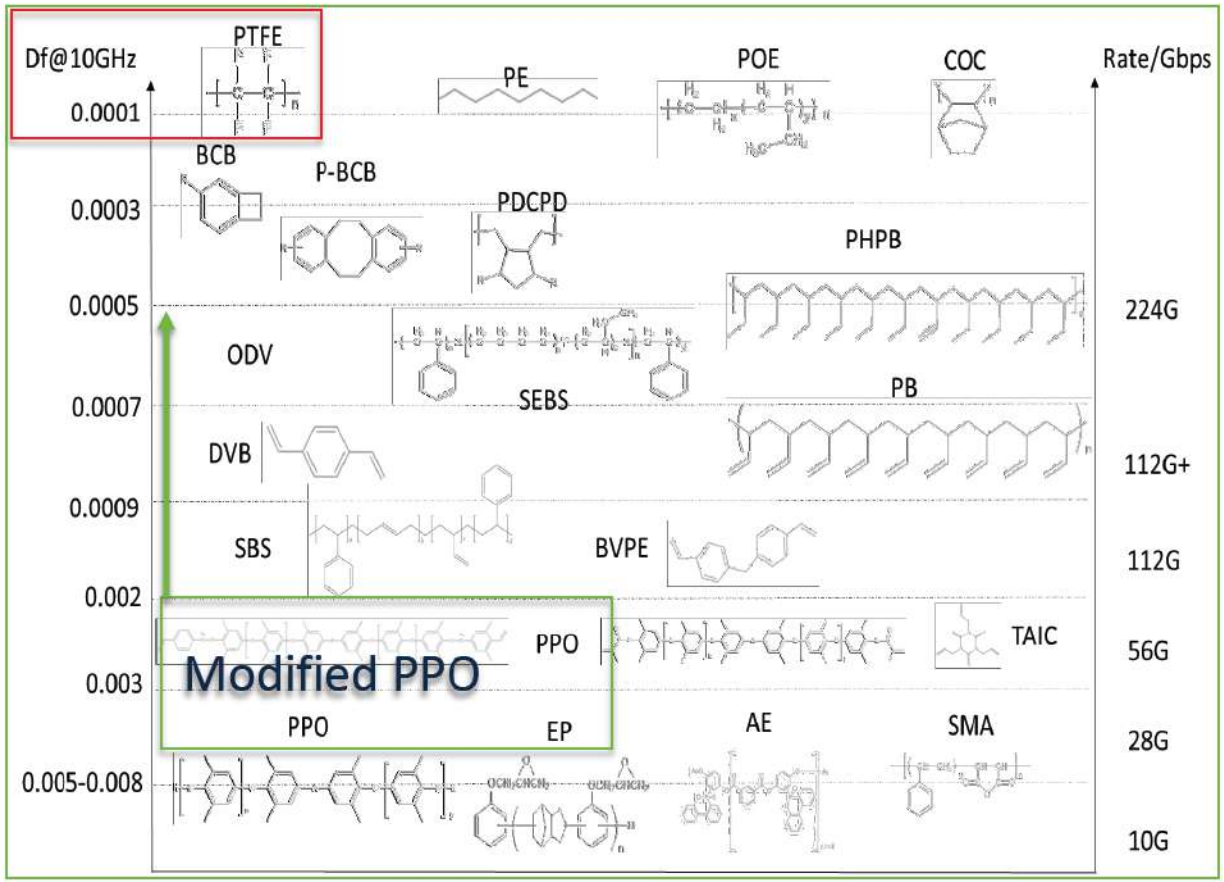
++PCB High-speed material evolution cycle become more and more shortly, faces huge challenge.

2-2 : 224G Ultra-low Loss PCB Solution , Scarlet Wang (Shengyi Technology) 외

Dielectric Resin Structural Formula and Df :

- **PTFE:** Polytetrafluoroethylene
- Df-0.0001@10GHz
- Extreme SI Performance
- Difficult in multilayer Production

- **Modified PPO:**
- Df-0.0006@10GHz
- Good SI Performance
- Good Multilayer Production



2-2 : 224G Ultra-low Loss PCB Solution , Scarlet Wang (Shengyi Technology) 외

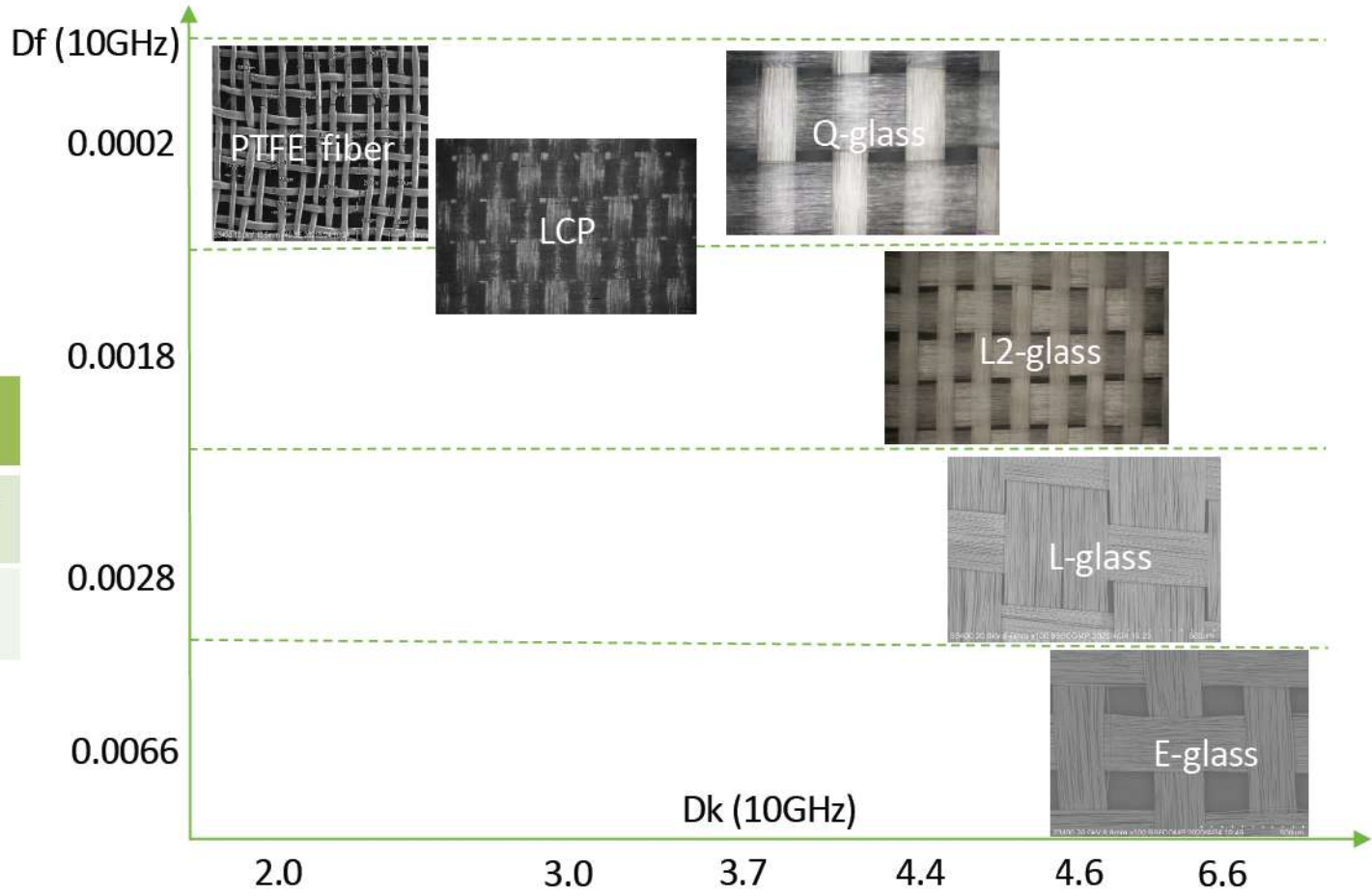
Reinforcement Material Types & Df :

- **PTFE/LCP Fiber**
- Low Df & Dk
- R&D stage

- **L2-glass/Q-glass for 224G**

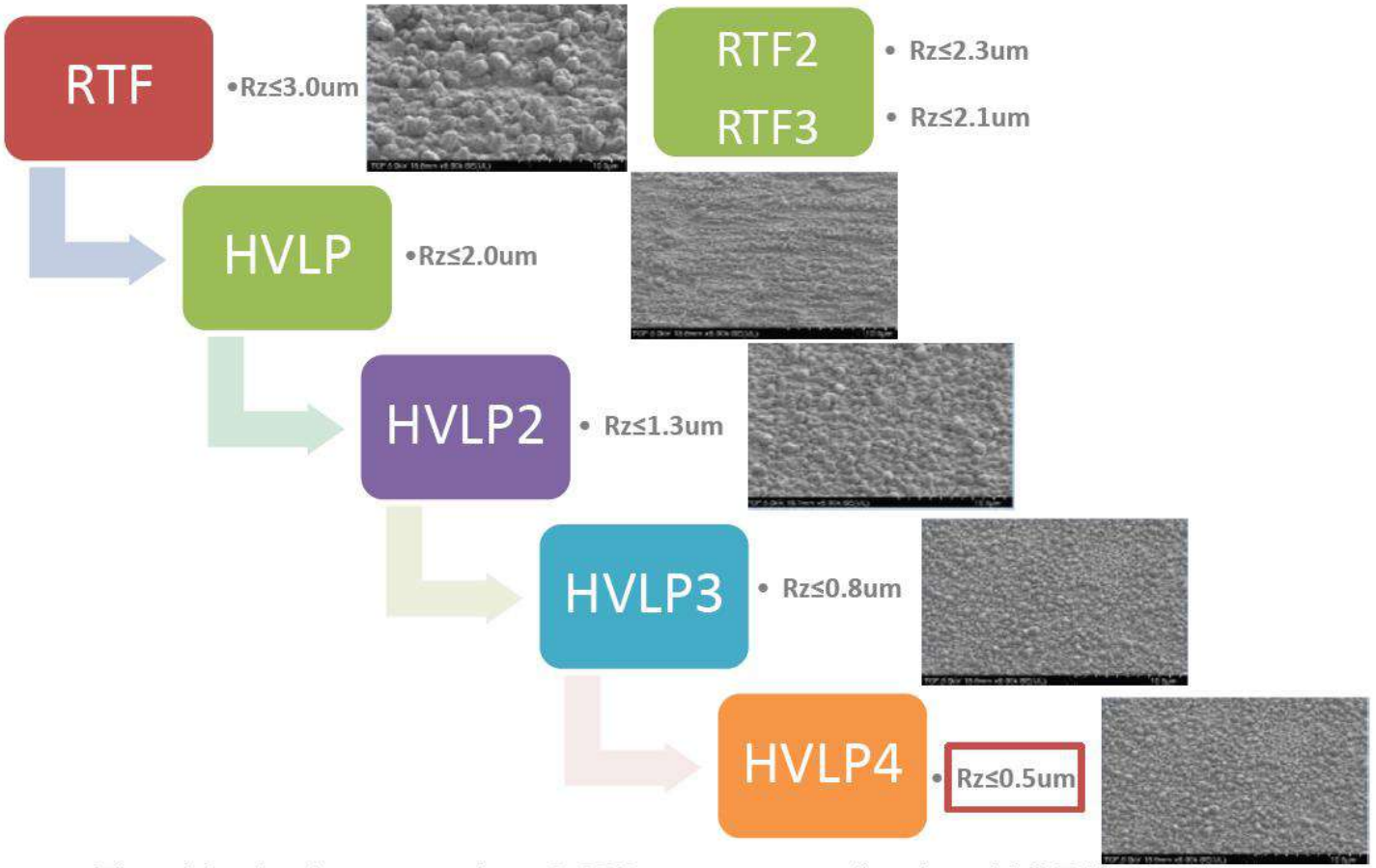
Glass Fiber	Capacity	source	cost
Q-glass	Not in MP	limited	Extremely high
L2-glass	Small qty.	limited	high

- **Low Dk glass**
- used in 56G/112G widely



2-2 : 224G Ultra-low Loss PCB Solution , Scarlet Wang (Shengyi Technology) 외

Copper Foil Roughness & Skin Depth :



$$\delta = \sqrt{\frac{1}{\pi . \sigma . \mu . f}}$$

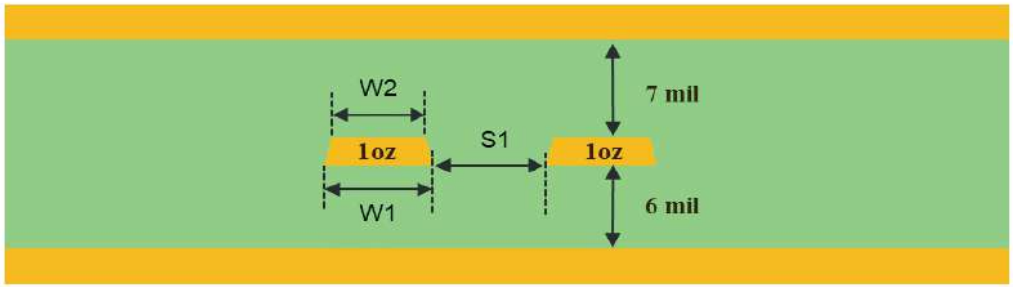
F (GHz)	0.1	1	10
δ (um)	6.497	2.055	0.65
F (GHz)	20	30	53
δ (um)	0.459	0.375	0.282

++The skin depth can reach to 0.282um, even smaller than HVLP4's roughness.
++ PCB oxidation process cannot go beyond 224G skin depth, considering loss performance improving, need lower

2. DesignCon 2024 자료 소개

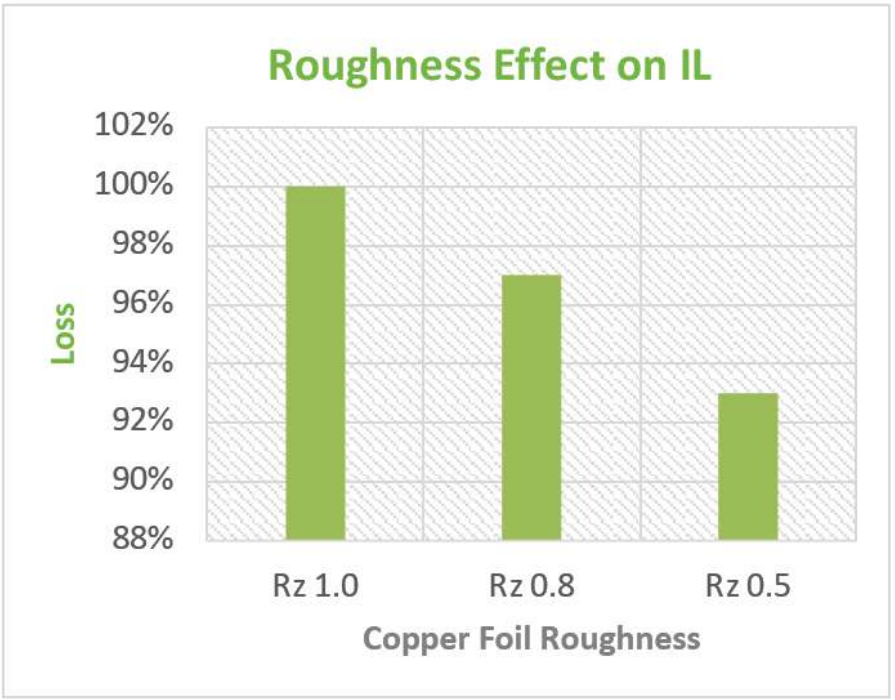
2-2 : 224G Ultra-low Loss PCB Solution , Scarlet Wang (Shengyi Technology) 외

Conductor Roughness Effect on IL :



7mil prepreg/ 6mil core Impedance: 92Ω Pitch (W+S): 14mil

Dielectric material	Copper foil thickness	Impedance design	Copper foil roughness
Dk 3.0 Df 0.0009	18um	92Ω	RZ=0.5μm (HVLP4)
			RZ=0.8μm (HVLP3)
			RZ=1.0μm (HVLP2)



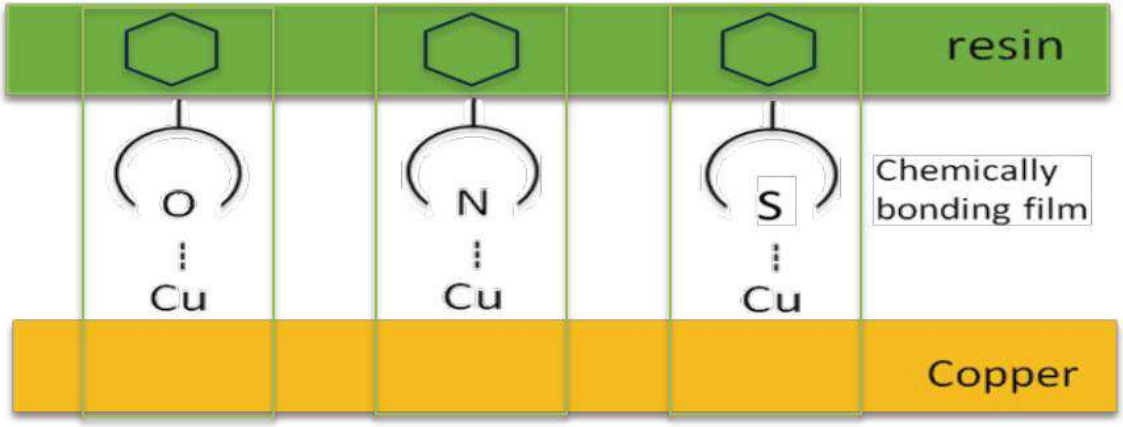
++Copper foil roughness Rz reduced from 1.0μm to 0.5μm, loss reduced of over 7%.
++The 224G high-speed material in this paper, chose new attempt: **modified PPO resin (Df <0.0006 @10GHz) without glass+ HVLP4**.

2-2 : 224G Ultra-low Loss PCB Solution , Scarlet Wang (Shengyi Technology) 외

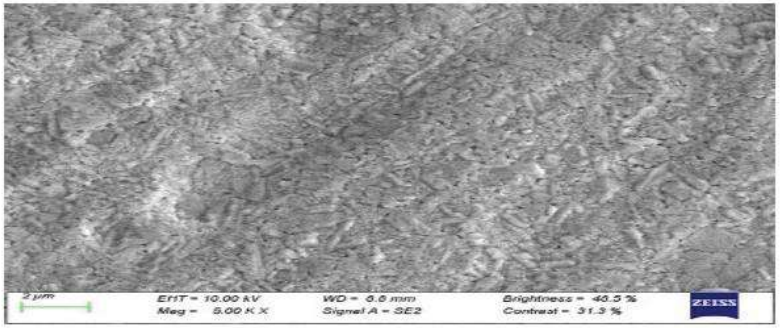
Brown Oxidation & Copper Foil Roughness :

Common PCB Brown Oxidation

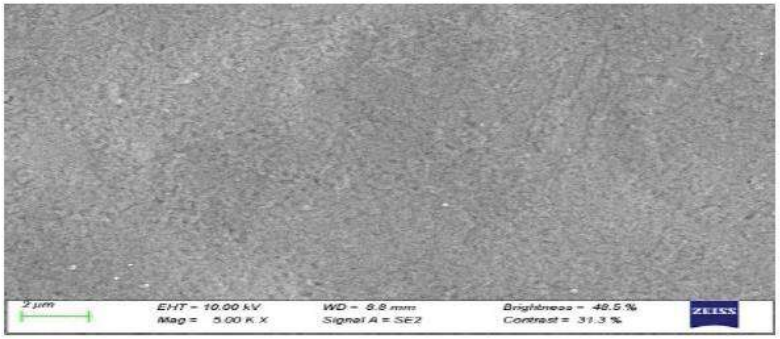
PCB Low Profile Brown Oxidation



Flattening + No-etching Oxidation



Original copper foil roughness Rsai=1.035

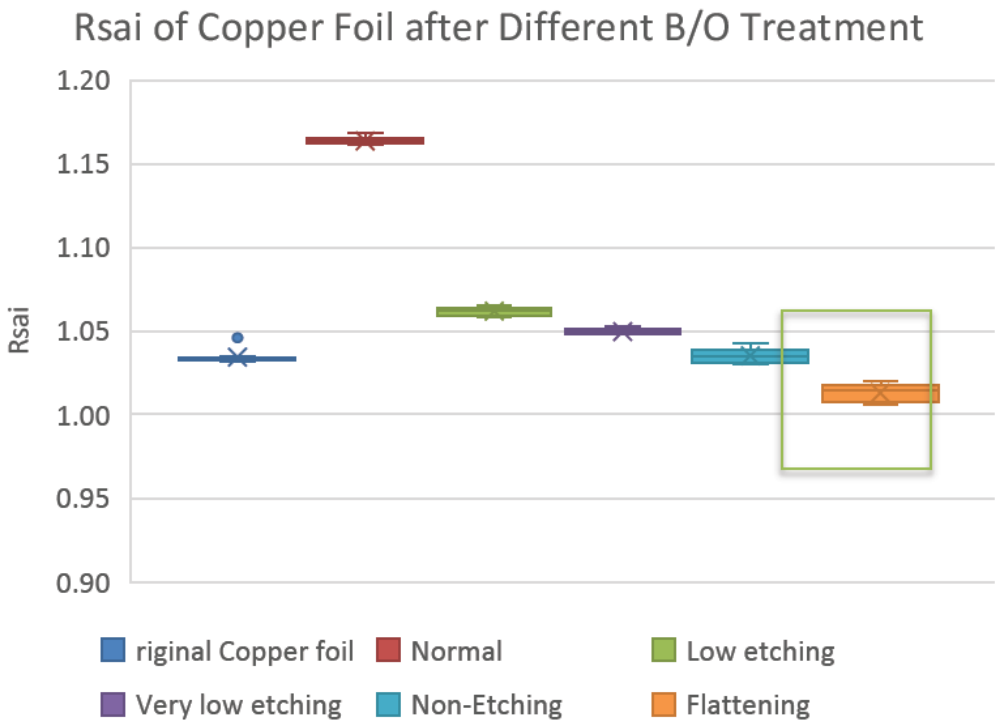


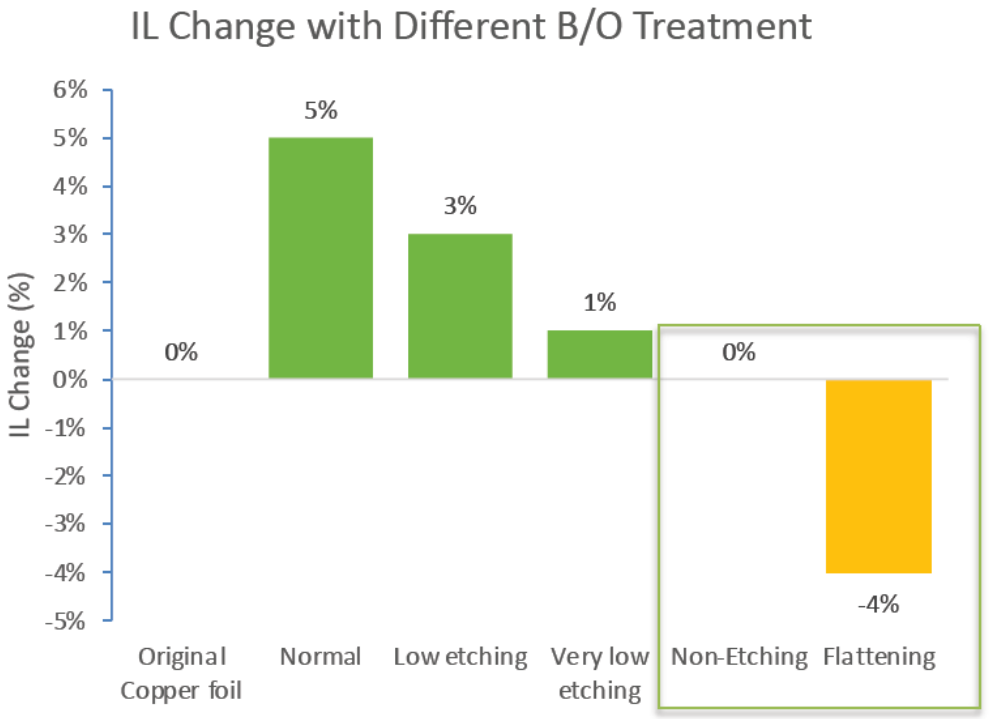
Flattening + No-etching roughness Rsai=1.013

++The copper foil roughness can reach to Rsai=1.013< original foil roughness and insure the bonding force by chemical bonding.

2-2 : 224G Ultra-low Loss PCB Solution , Scarlet Wang (Shengyi Technology) 외

Brown Oxidation & Insertion Loss :





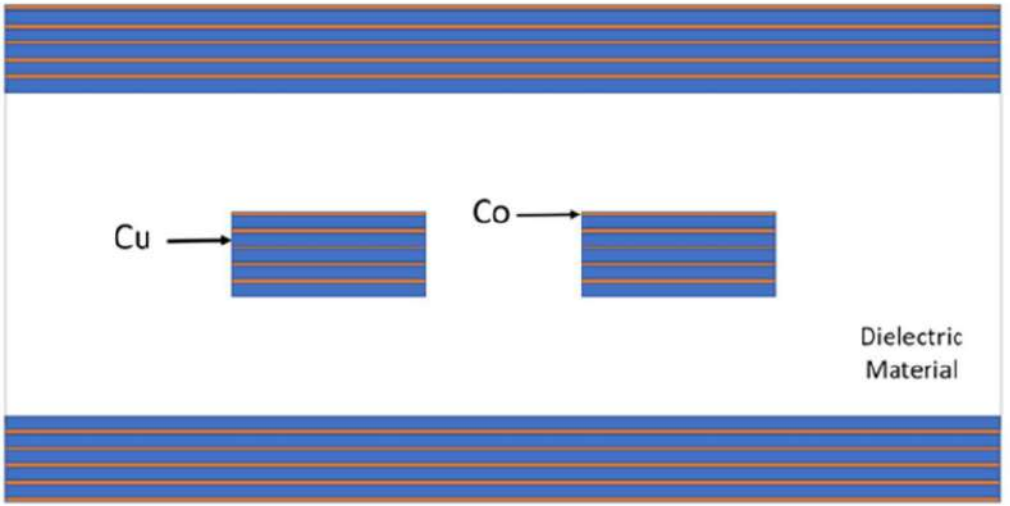
++ Flattening + no-etching roughness Rsai=1.013, IL performance better than original copper foil and any other previous PCB oxidation process.

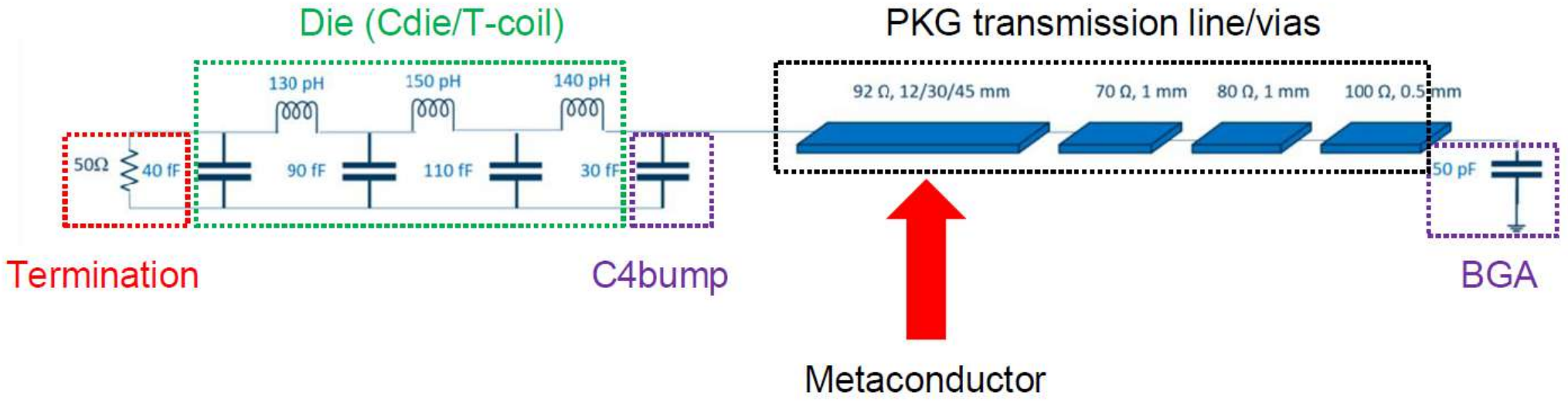
2. DesignCon 2024 자료 소개

2-3 : Enhancing End-to-End 224G Systems by Optimizing Metaconductors for Package Performance , Montserrat Benito-Villafranca (Marvell) 외

Metaconductors :

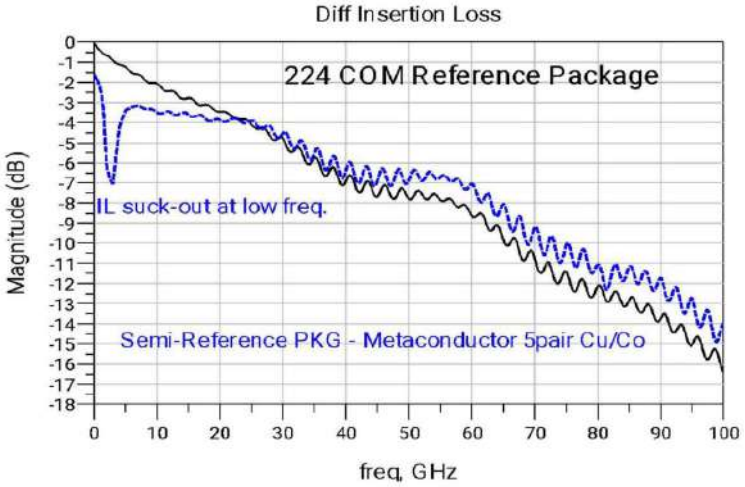
Channel Operating Margin (COM) :

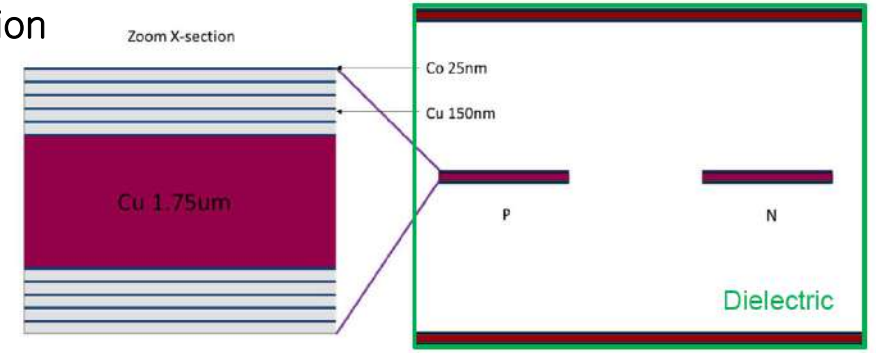


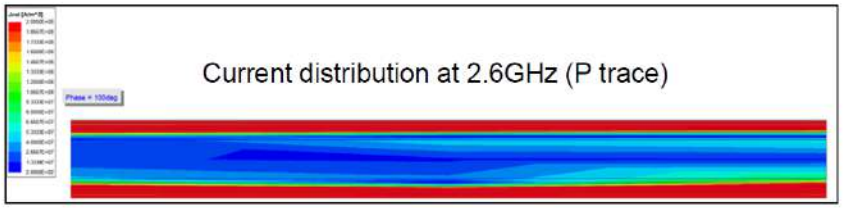


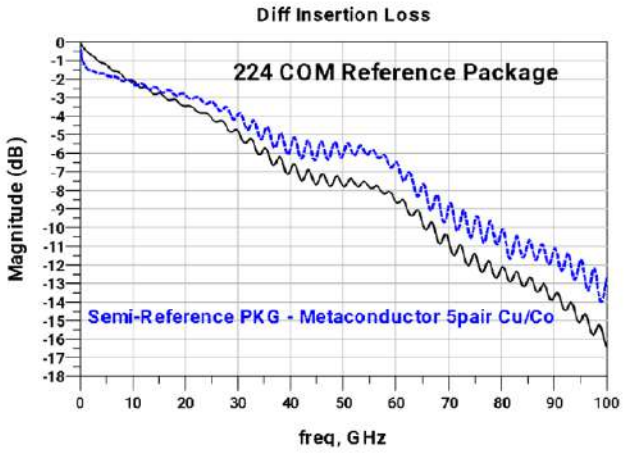
2-3 : Enhancing End-to-End 224G Systems by Optimizing Metaconductors for Package Performance , Montserrat Benito-Villafranca (Marvell) 외

Metaconductors : Problem Statement => Coplanar Solution









DUT	COM (dB)
20dB Backplane Channel with reference package	-2.35dB
20dB Backplane Channel with the semi-reference package with meta-conductor (version 2)	-0.2dB

2. DesignCon 2024 자료 소개

2-3 : Enhancing End-to-End 224G Systems by Optimizing Metaconductors for Package Performance , Montserrat Benito-Villafranca (Marvell) 외

Takeaways and Conclusions :

- We have introduced a new metric to study 224G end-to-end channels by incorporating Cu/Co metaconductors on coplanar packages. The foundation design of alternating Cu/Co structures produced a severe IL suck-out at low frequency, which negatively impacted the overall performance. To address this issues, a novel solution has been implemented to eliminate the IL suck out.

- COM results have demonstrated that the implementation of coplanar metaconductor technology may provide benefits in end-to-end 224G Ethernet systems. The weighting factor assigned to packages in the allocated end-to-end channel insertion loss budget can be as high as 40% of the total channel loss. Consequently, the benefit of reducing and flatting the IL profile on packages can have a significant impact on reducing the pulse dispersion response.

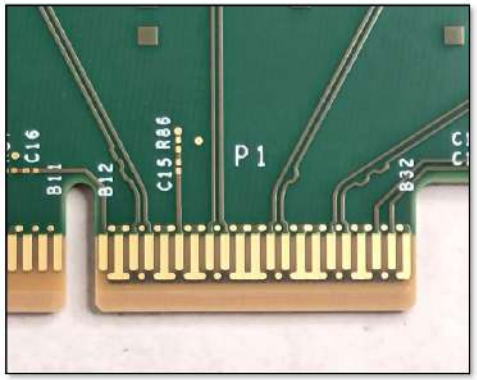
- Future work includes analyzing the impact on current equalization schemes, specifically FFEtx and DFErx. Additionally, finding alternative ferromagnetic thin film or different thicknesses to produce negative permeability up to 60GHz that will enhance the PKG performance.

2-4 : PCI Express & PAM4: The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems , Pegah Alavi(Keysight Technologies) 외

PCIe 7.0 : What is coming => Modeling , Simulation Challenges

- **Data Rate: 128 Gb/s (PAM4)**
- **BER: 1e-6**
- **SNDR: 34 min (same as PCIe 6.0)**
- **RLM: 0.95 min (same as PCIe 6.0)**
- **Channel: 4” – 14” (similar to PCIe 6.0)**
  - Loss -36dB to -40dB
- **Tx equalization (Proposed)**
  - 4-tap FIR
- **Rx equalization (Proposed)**
  - Reference CTLE (6poles, 3 zeros, gain range 0 to -20dB)
  - ADC based Rx Architecture (FFE with 24 post-cursor and 4 pre-cursor taps, + 1-tap DFE)
  - h1/h0 < 0.5
- **Rx eye mask (TBD)**

Physical Form Factor Updates – CEM Card



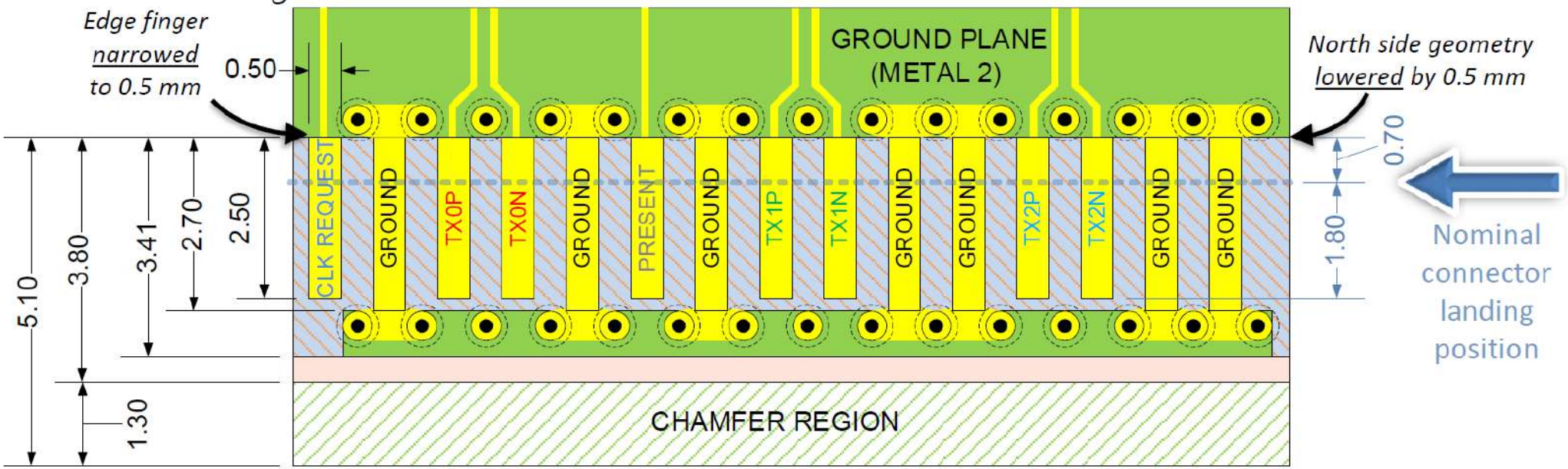
PCIe CEM 6.0 edge finger design

- **Rev 6.0 of the PCIe Card Electromechanical (CEM) form factor specification reached its 0.7 maturity**
- **CEM 6.0 introduces updates to edge finger PCB layout for the Add-in Card edge finger geometry to improve signal integrity extending to 64.0 GT/s**
- **Largely extends connector baseboard footprint and Add-in Card geometry updates introduced in PCIe 4.0 and 5.0**
- **Early pathfinding is underway for 128 GT/s PCIe CEM 7.0**

2-4 : PCI Express & PAM4: The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems , Pegah Alavi(Keysight Technologies) 외

CEM Add-in Card edge finger geometry updates :

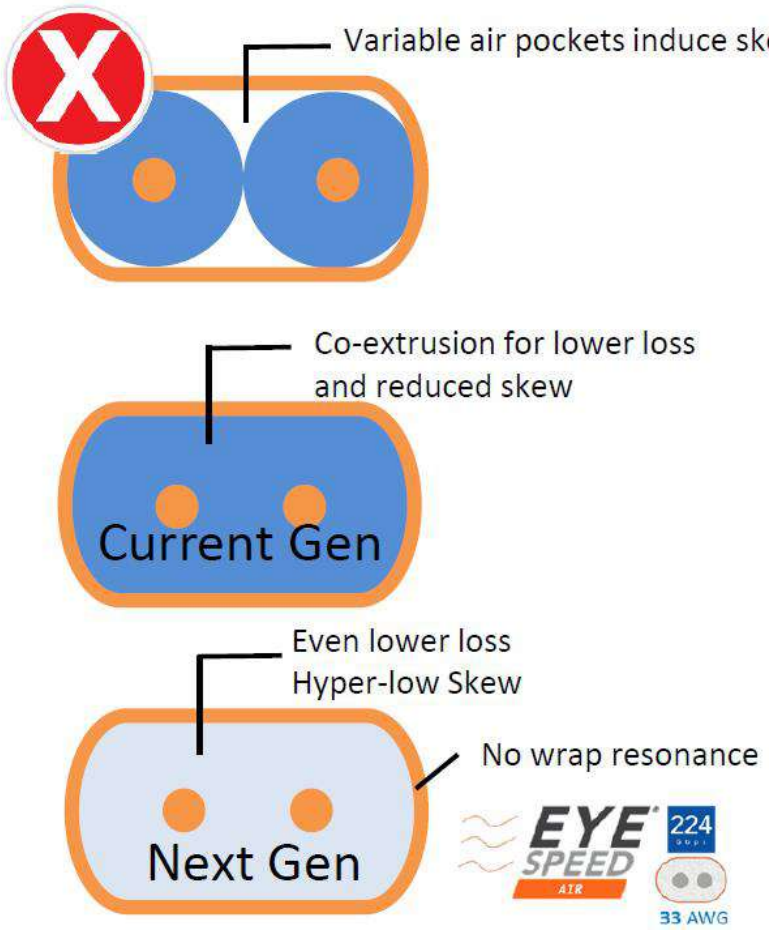
- **CEM 6.0 Edge finger region introduces the "Low North" and narrower, 0.5 mm fingers**
  - Moves the geometry on the upper end of the edge finger region ↓South↓ by 0.5 mm
  - Edge finger lengths are reduced by 0.5 mm, *but the 1.8 mm stub length remains unchanged*

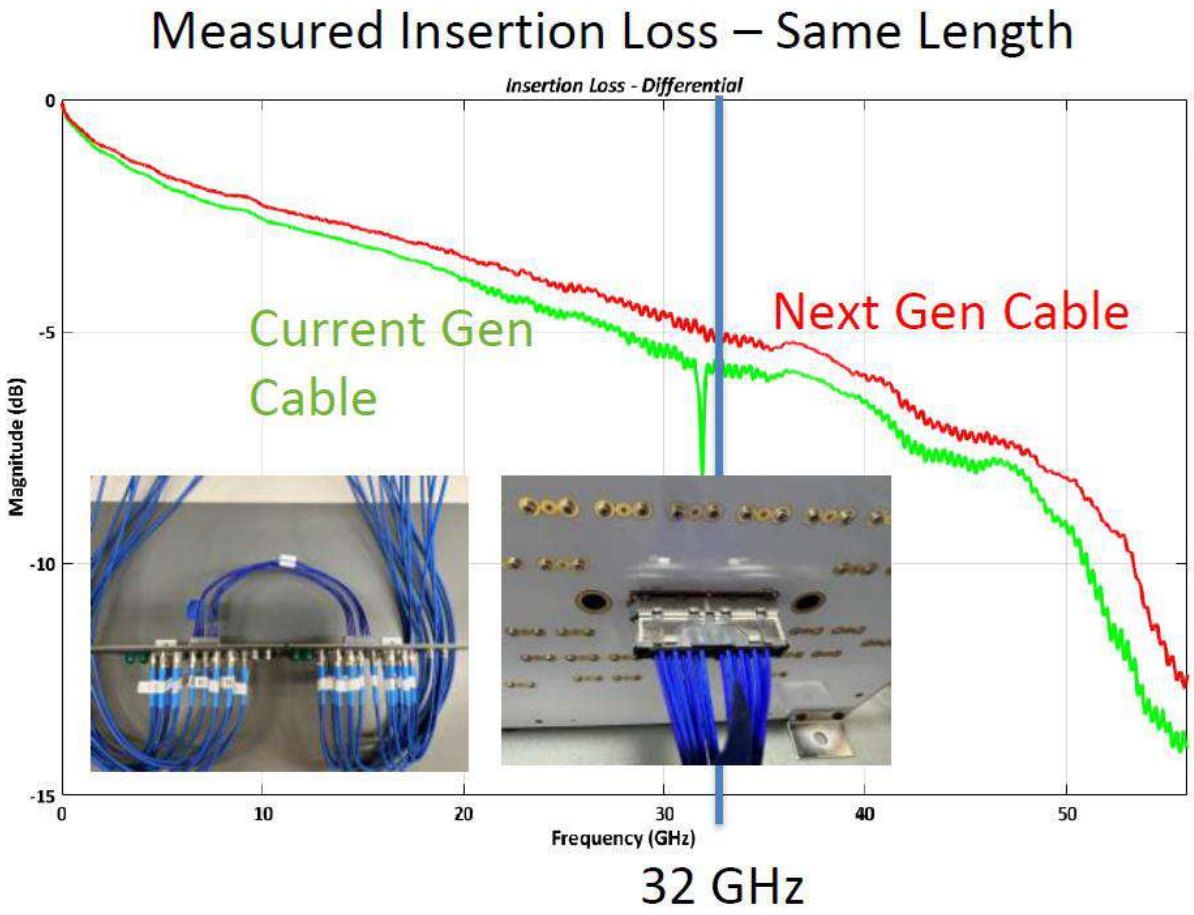


2. DesignCon 2024 자료 소개

2-4 : PCI Express & PAM4: The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems , Pegah Alavi(Keysight Technologies) 외

Cable Pathway to Gen 7 128GT/s :





2-4 : PCI Express & PAM4: The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems , Pegah Alavi(Keysight Technologies) 외

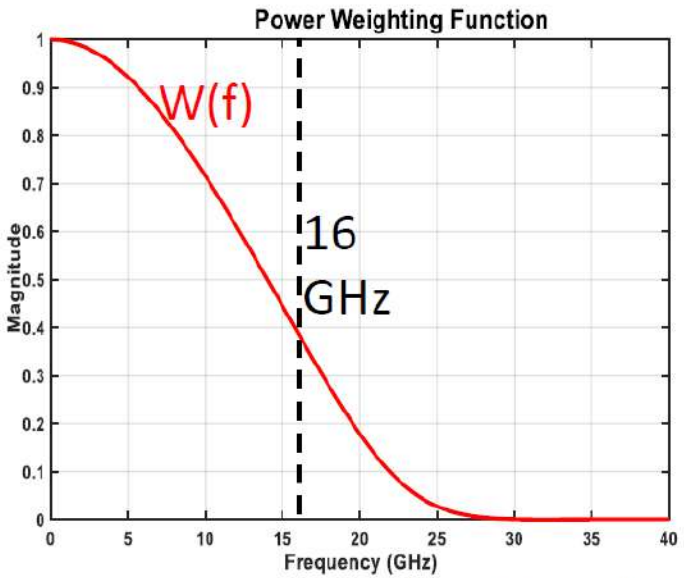
Integrated Return Loss (IRL) :

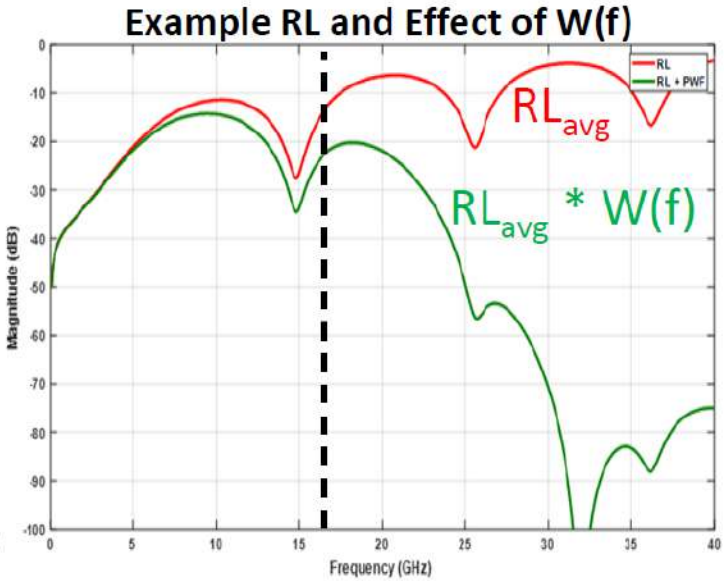
The Problem

- Connectors\Cables slightly exceed RL limit
- System still works
- False negative

The Solution

- IRL approves excursions that would still “work”
- Return Loss is filtered by W(f), and then integrated
- Like ICN for crosstalk





$$W(f_i) = sinc^2(f_i/f_b)\left(\frac{1}{(1+(f_i/f_t)^4)}\right)\left(\frac{1}{(1+(f_i/f_r)^8)}\right)$$

$$RL_{avg}(f_i) = (|RL_{11}(f_i)| + |RL_{22}(f_i)|)/2$$

$$iRL = dB\left(\sqrt{\frac{1}{N}\sum_{i=1}^{N} W(f_i)\, RL_{avg}^2(f_i)}\right)$$

May appear in CEM 6.0 and internal\external cable 5.0 and 6.0

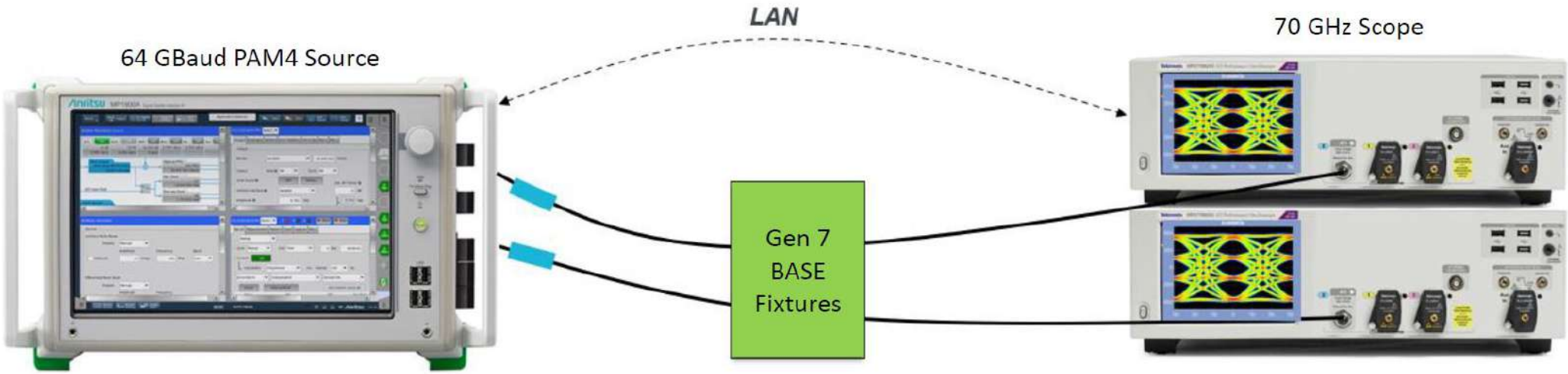
2-4 : PCI Express & PAM4: The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems , Pegah Alavi(Keysight Technologies) 외

Receiver Validation Evolution :

	PCIe 5.0	PCIe 6.0	128 GT/s (TBD)
Max data rate	32Gb/s	64GT/s (32Gbaud PAM4)	128GT/s (64Gbaud PAM4)
Channel loss range	-34 to -37dB @ 16GHz	-30 to -33dB @ 16GHz	~ 36dB @ 32GHz
Add-in card loss	9.5dB @ 16GHz	8.5dB @ 16GHz	~ 9dB @ 32GHz
Reference CTLE	4 poles, 2 zero, DC gain range -5 to -15dB	6 poles, 3 zero, DC gain range -5 to -15dB	6 poles, 3 zero, DC gain range 0 to -15dB (gain)
Reference DFE / FFE	3-tap DFE	16-tap DFE	~ 28-tap FFE & 1-tap DFE
Eye width (RX test)	9.375 ps	3.125 ps (top eye)	TBD
Eye height (RX test)	15 mV	6 mV (top eye)	TBD
Lane margining	Timing and voltage	Timing and voltage	Expected

2-4 : PCI Express & PAM4: The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems , Pegah Alavi(Keysight Technologies) 외

128 GT/s (PAM4) Stressed Eye :



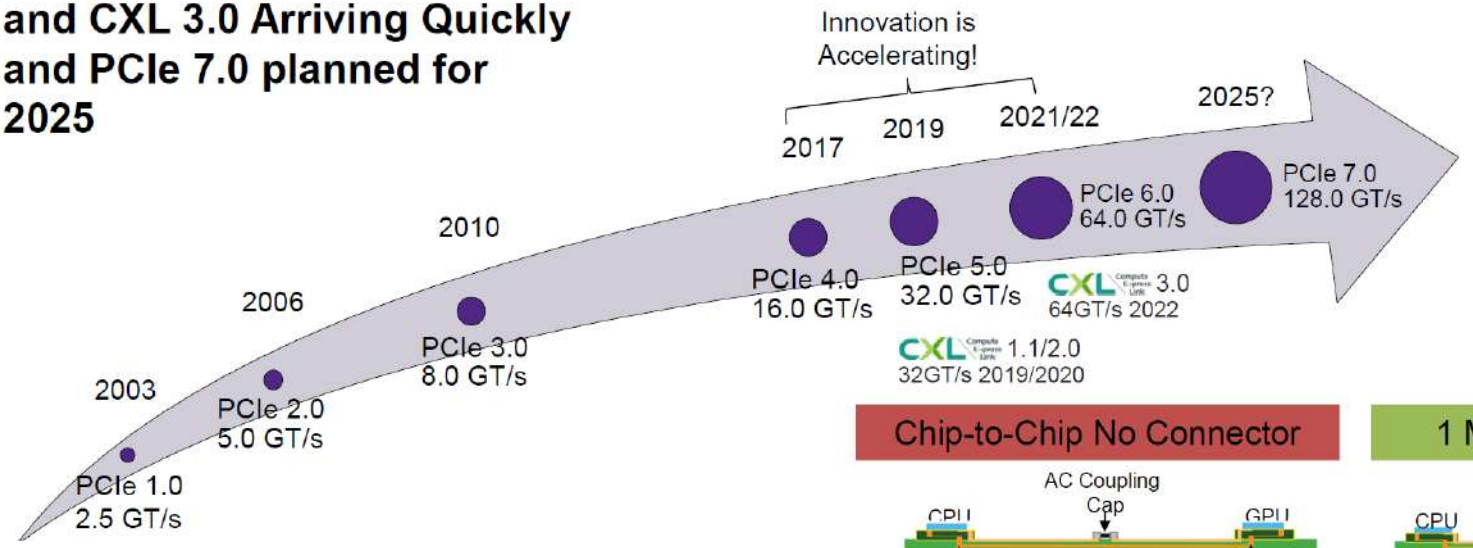
- **Source:** PAM4 PPG
  - 128 GT/s (64 GBaud PAM4) – Step Response
  - Tx EQ Presets: Gen6 Presets?
- **Channel:** ~ 36dB @ 32 GHz
  - Available Variable ISI boards

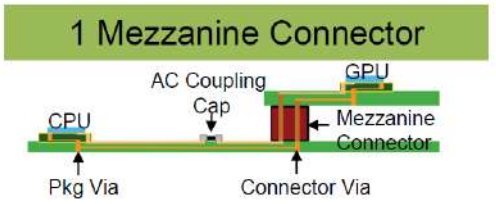
- **Scope:** Real Time Oscilloscope
  - ~65 to 70 GHz with lower BT filter expected
- **Post Processing:** Seasim 2.0.96
  - CTLE/FFE/DFE
  - Sj, Rj, & Crosstalk (DMI) to be explored
  - Instrument noise compensation likely

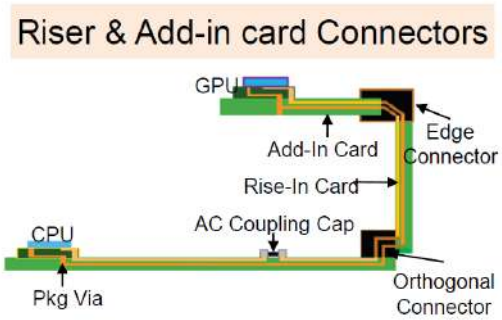
2-4 : PCI Express & PAM4: The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems , Pegah Alavi(Keysight Technologies) 외

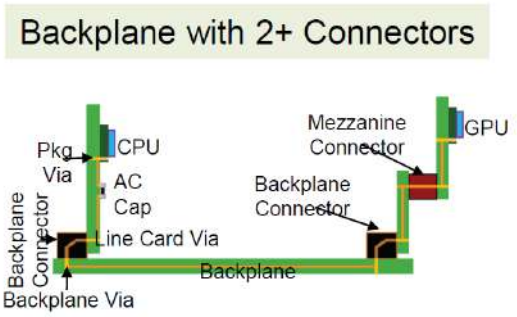
PCI Express Specifications are Accelerating :

- **Innovation is Accelerating since PCIe 3.0, with PCIe 6.0 and CXL 3.0 Arriving Quickly and PCIe 7.0 planned for 2025**









2-5 : Mitigating crosstalk through the placement of Power-Ground Capacitors for DDR5 Memory , Pratik Khurana (Achronix Semiconductor Corporation) 외

Crosstalk Failing the Specification :

- **Power-sum Crosstalk @5600 Mbps for signals routed on L03 layer.**
- **Power-sum crosstalk for DQ24 to DQ29 as victim and multiple other aggressors.**
- **Spike @300MHz in PSNEXT and PSFEXT.**

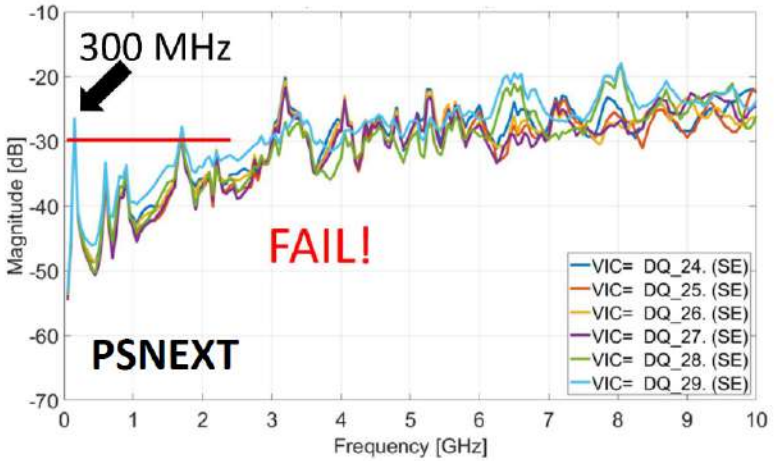


Figure. Power-sum Near-end Crosstalk.

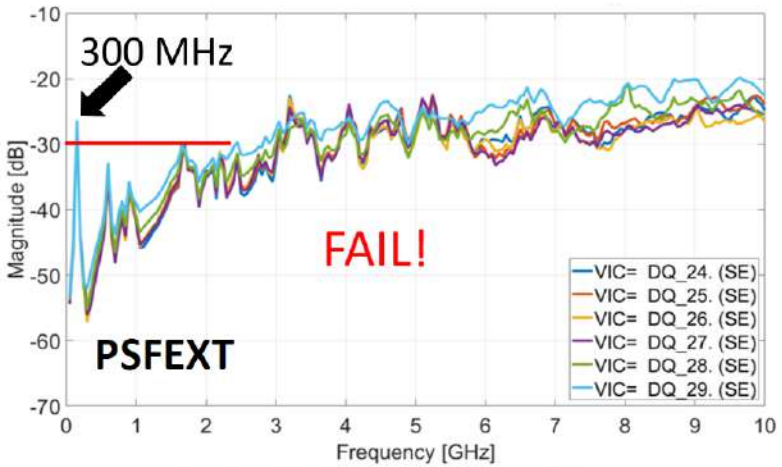


Figure. Power-sum Far-end Crosstalk.

2. DesignCon 2024 자료 소개

2-5 : Mitigating crosstalk through the placement of Power-Ground Capacitors for DDR5 Memory , Pratik Khurana (Achronix Semiconductor Corporation) 외

Proposal: PWR-GND capacitors at DIMM

- Placements of PWR-GND capacitors on right side of DIMM connectors for both Single and Dual-DIMM configuration.
- Twenty-two 0402 Capacitors are used of 0.1uF value.

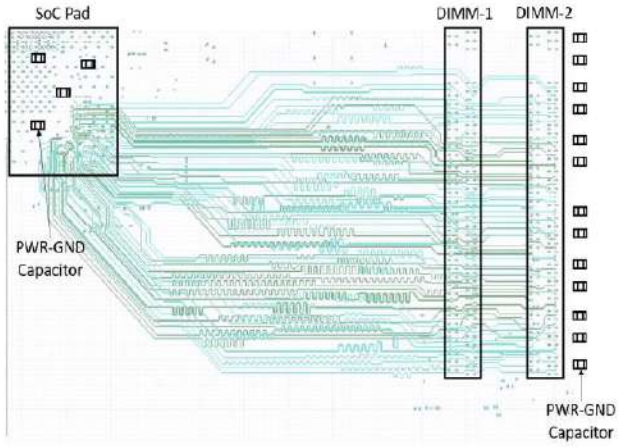


Figure. Dual-DIMM Configuration.

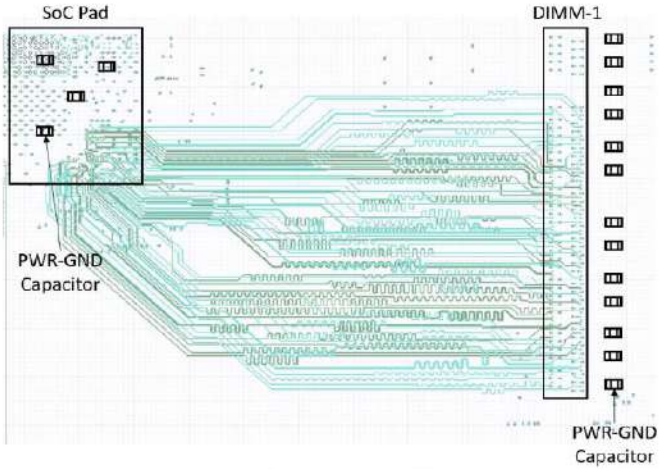


Figure. Single-DIMM Configuration.

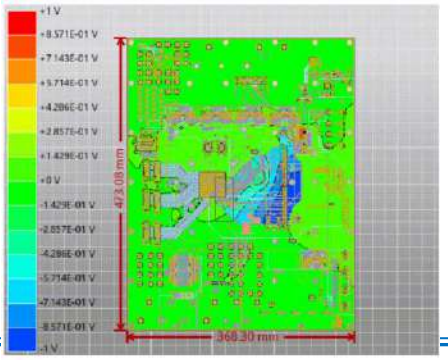


Figure. Voltage distribution across layer 02 at 300MHz.

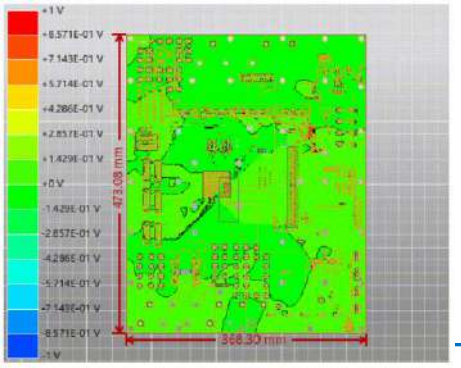
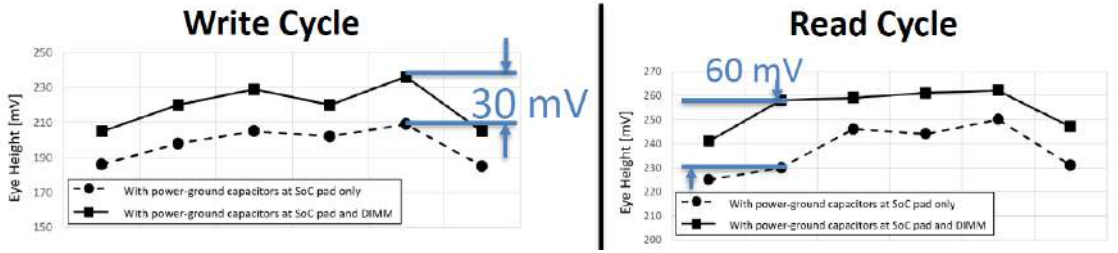


Figure. Voltage distribution across layer 02 at 300MHz.

2. DesignCon 2024 자료 소개

2-5 : Mitigating crosstalk through the placement of Power-Ground Capacitors for DDR5 Memory , Pratik Khurana (Achronix Semiconductor Corporation) 외

Results :



- Full wave EM- Extraction using lumped capacitors have significant effect.
- Improvement of Power-sum Near-end and Far-end Crosstalk after placing the PWR-GND Capacitors near DIMM connector.
- Spikes at lower frequency around 300MHz have suppressed.

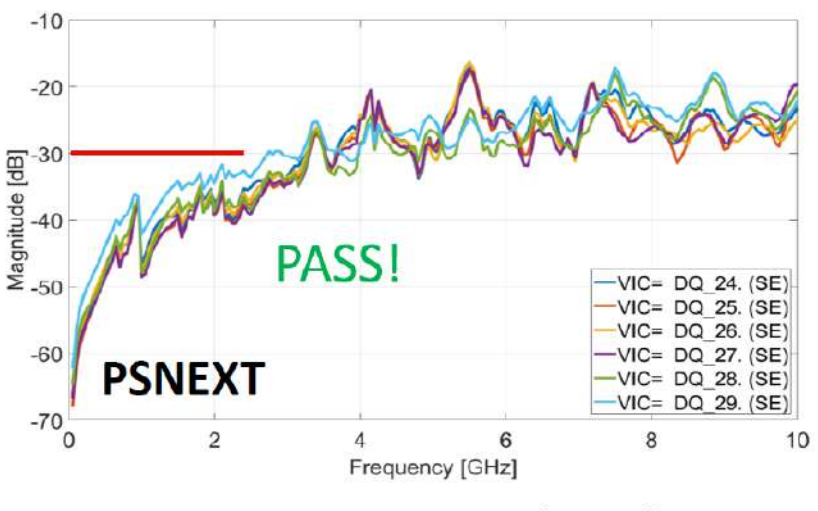


Figure. Power-sum Near-end Crosstalk.

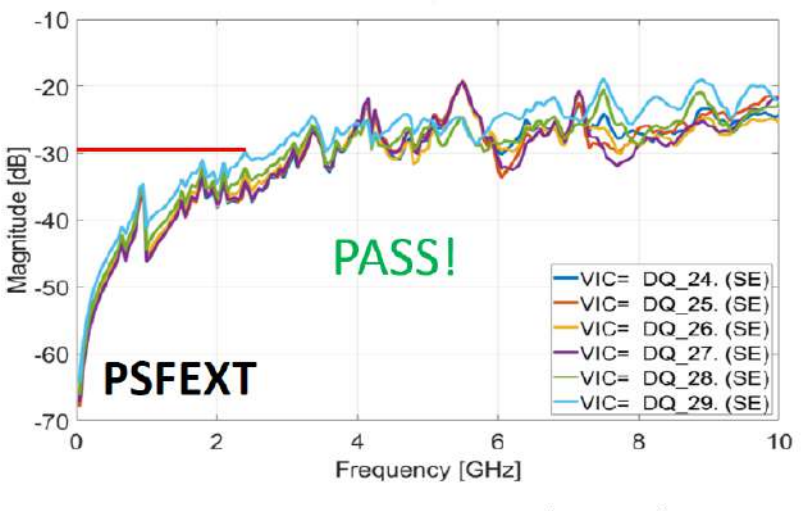
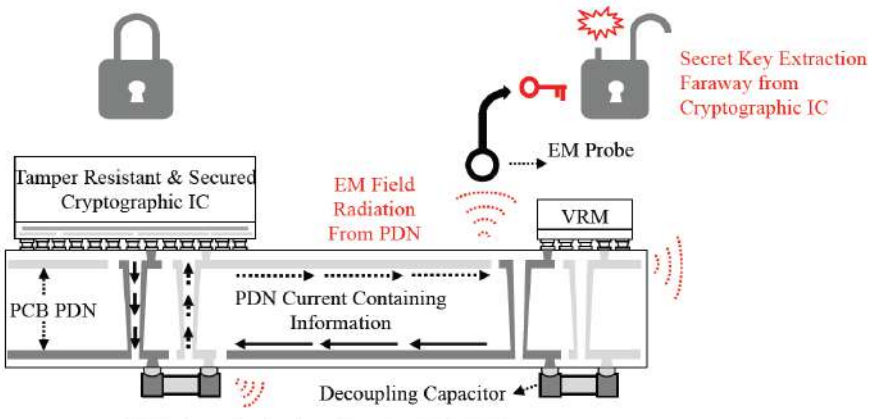


Figure. Power-sum Far-end Crosstalk.

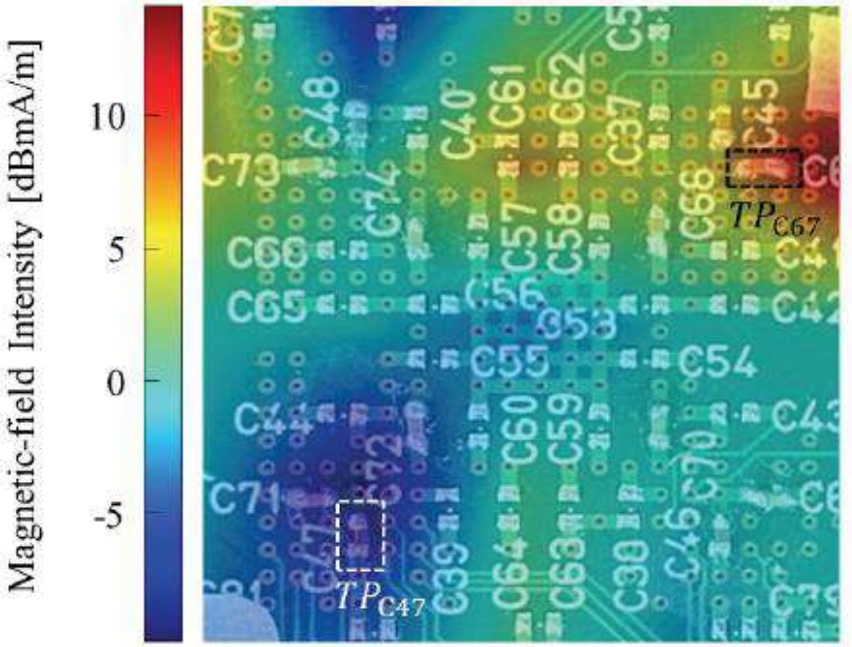
2. DesignCon 2024 자료 소개

2-6 : EMI and Intentional-EMI Attacks against Power Delivery Network of Crypto/Information Devices , Youngwoo Kim, Sejong University

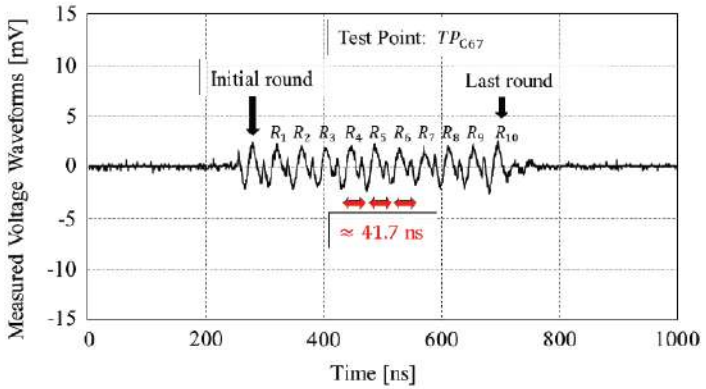
Unprotected PCB PDN => EM information leakage issues



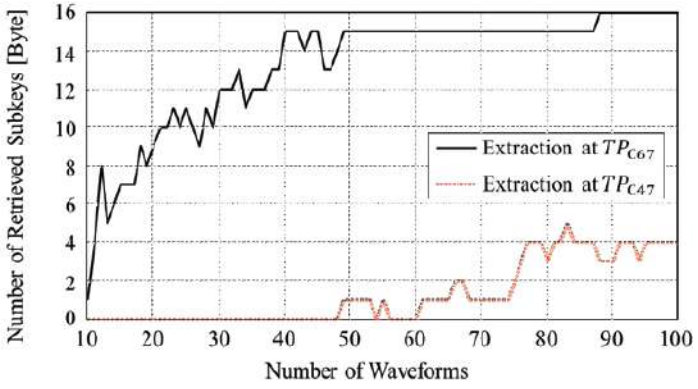
<EM information leakage from the PCB PDN>



- Since operation frequency of the cryptographic device is relatively low, current in the PCB PDN resembles the chip current.
- As a result, radiation from the PCB PDN can cause EM information leakage issues



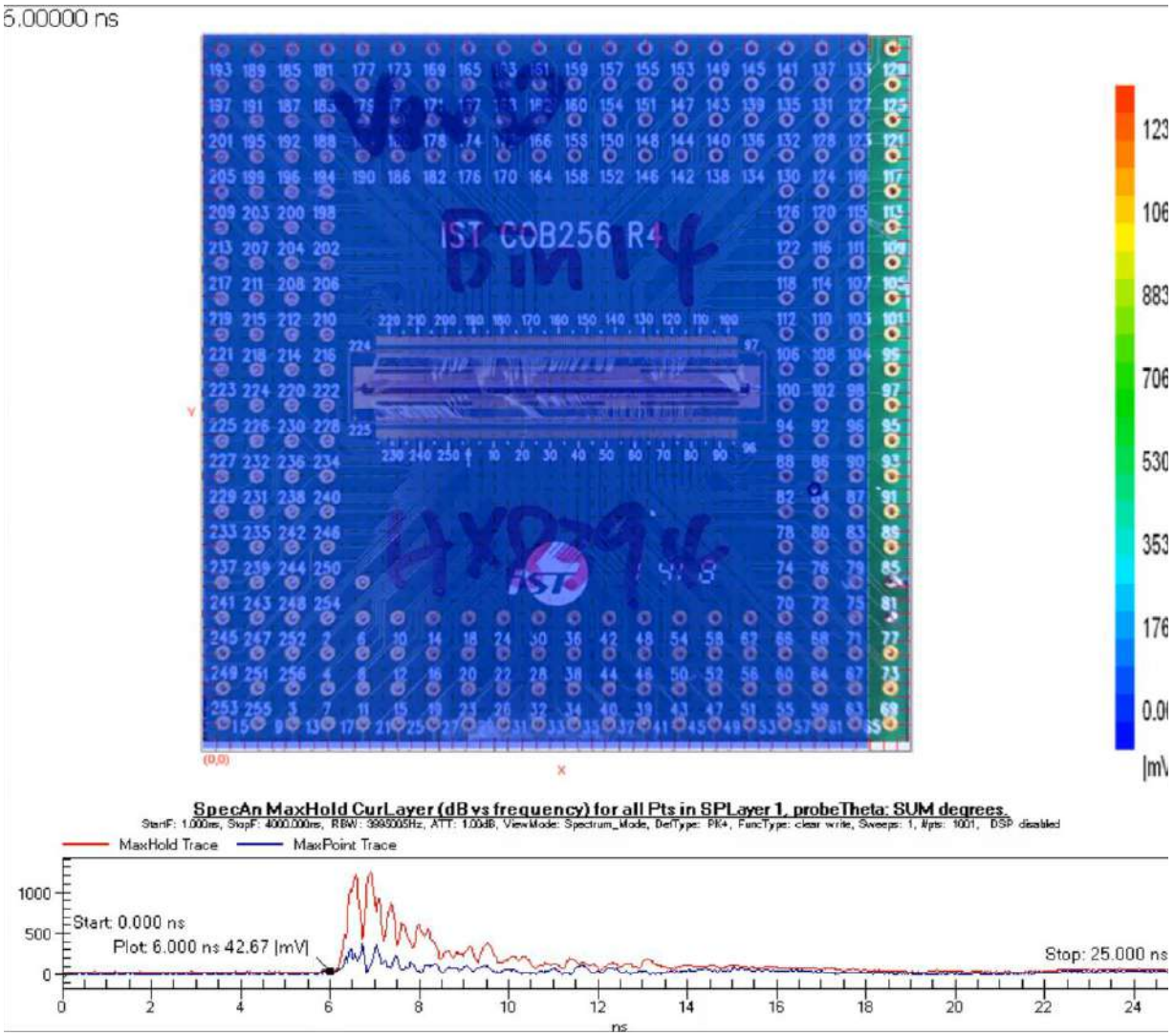
< Crypto-activity is clearly visible >

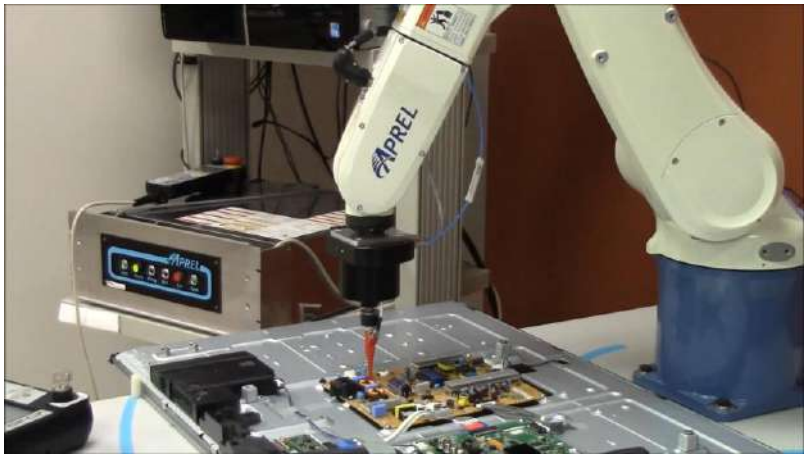


< Key extraction test>

* Chip level EMI : APPREL measurement (Huwin)

Chip level EMI near field scan measurement (time & frequency) and simulation

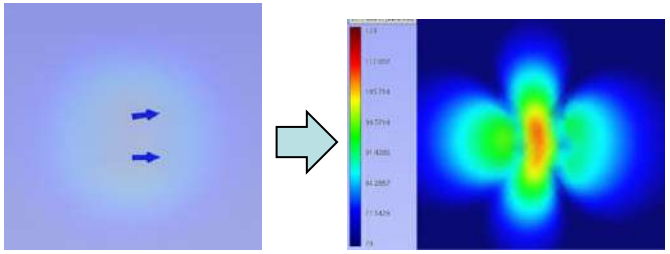




Single Vector probe solution from 9kHz to 50GHz

High resolution scan (>0.01/0.07 mm) based on system, full 360 degree Vector probe rotation

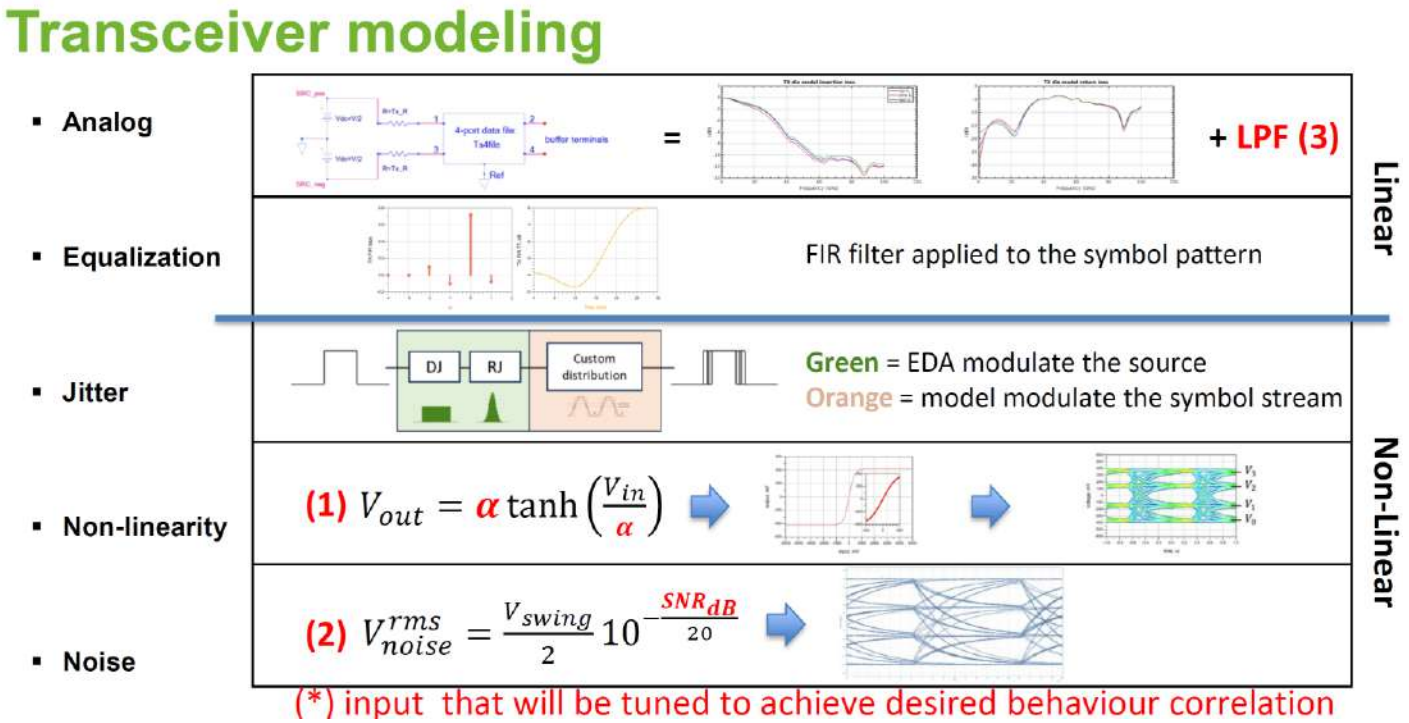
Vector Near Field source => HFSS, EMCoS Simulation 가능



Reconstruction dipole
By Near-field data measured at 4 mm

2-7 : Correlation methodology for 128 GT/s operation of PCIe ® 7.0 DSP-based IBIS-AMI models , Adrien Auge (Alphawave Semi) 외

PCIe 7.0 PAM4 Transmitter modeling 및 검증 :

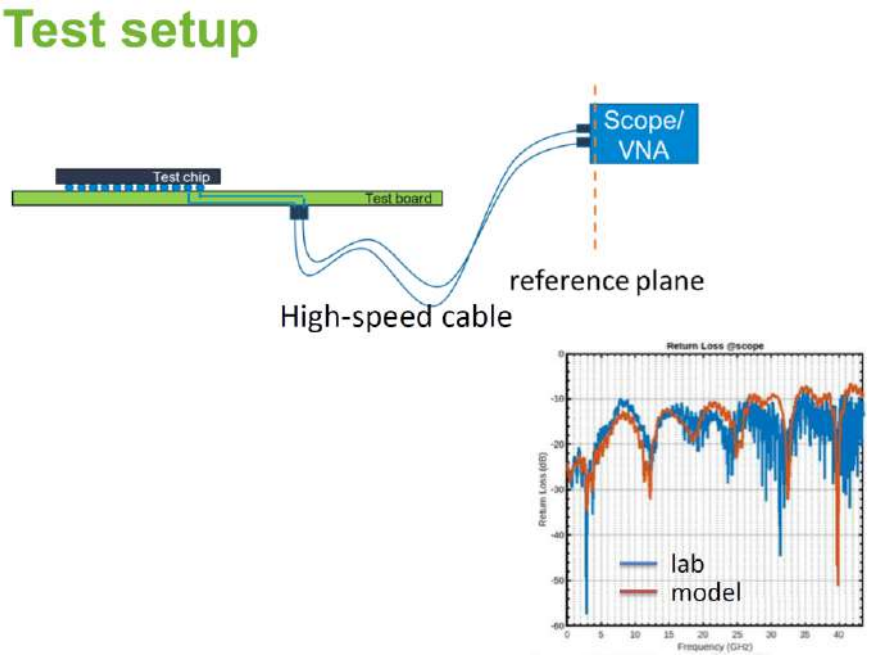


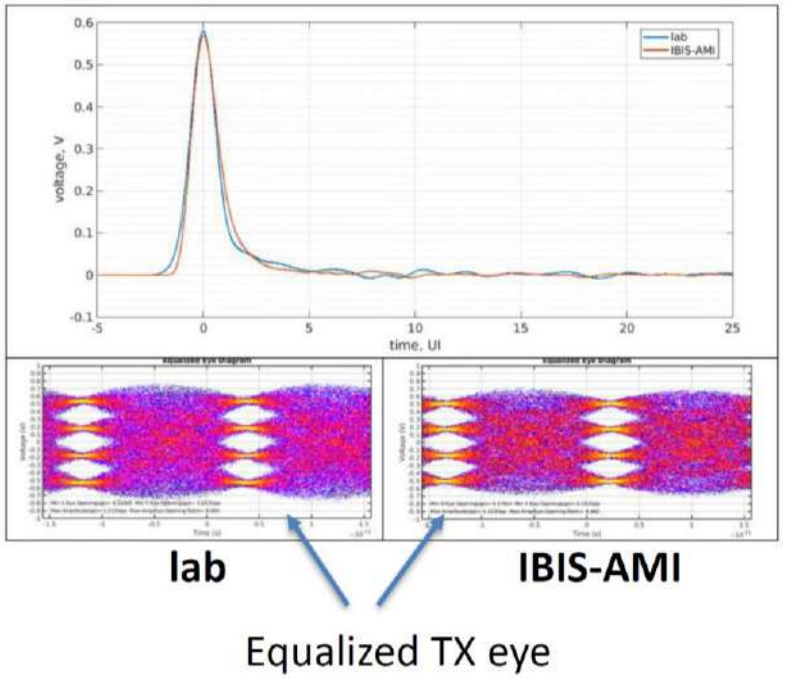
① Analog: post-layout parasitic simulation 통하여 추출
② Linear EQ: FIR filter 적용
③ Non-linearity: tanh()을 이용하여 신호 크기 compression
④ Noise: RMS noise

2. DesignCon 2024 자료 소개

2-7 : Correlation methodology for 128 GT/s operation of PCIe ® 7.0 DSP-based IBIS-AMI models , Adrien Auge (Alphawave Semi) 외

PCIe 7.0 PAM4 Transmitter modeling 및 검증 :





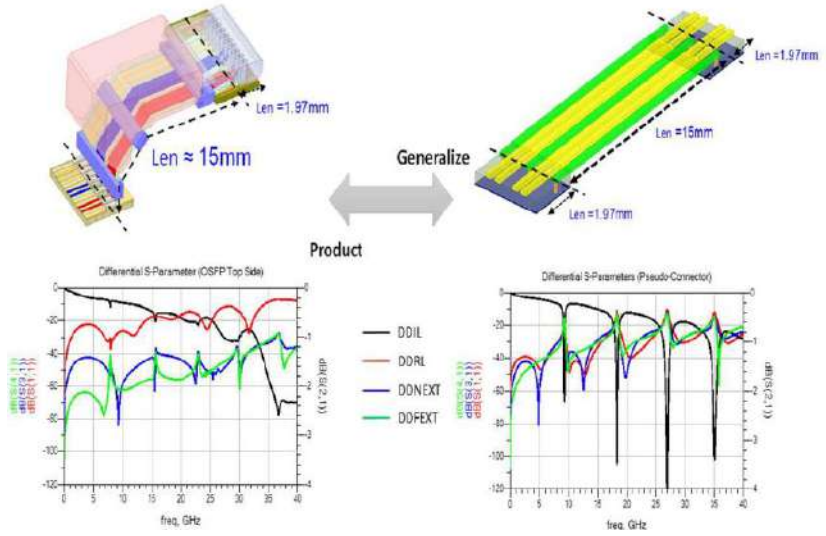
① Passive channel (fixture+cable): bare substrate pkg이용하여 측정
② Analog model + Passive channel 의 Return loss 측정과 비교 (Return loss)
③ Waveform 출력 결과로 부터 Linear + Non-linear + Noise 파라미터 도출

2. DesignCon 2024 자료 소개

2-8 : m-TL Circuit Model of 5/6G Connectors for Fast Resonance Crosstalk Analysis, Yulin He (University of Illinois at Urbana-Champaign) 외

Connector의 1D model 생성을 통한 SI 성능 최적화 속도 개선 :

Connector model **Baseline model**



등가 모델 추출

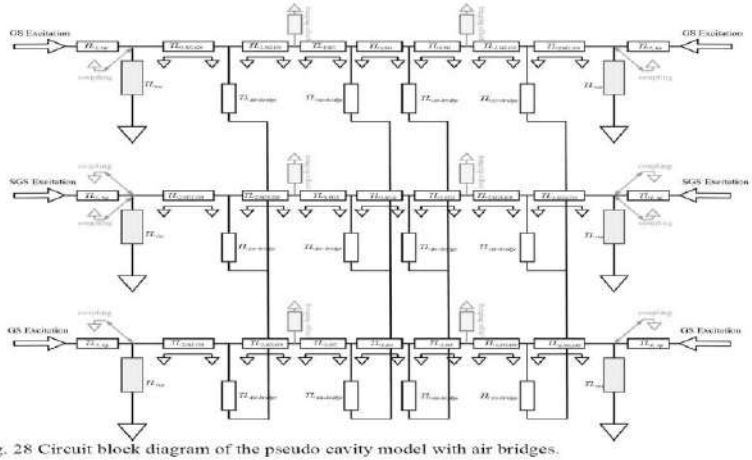


Fig. 28 Circuit block diagram of the pseudo cavity model with air bridges.

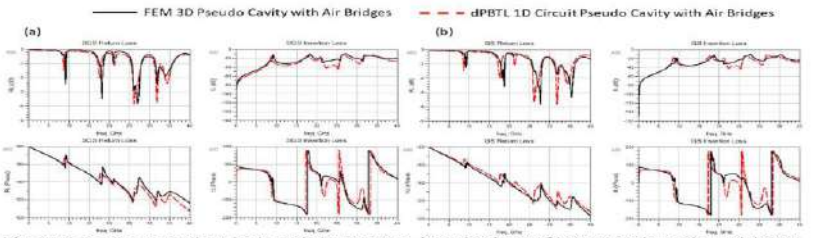


Fig. 29 S-parameter results (single-ended return loss, insertion loss) of FEM Pseudo-cavity and dPBTL equivalent circuit on (a) S-G-S air-bridged resonator and (b) S-G air-bridged resonator, ports at S-G-S and S-G respectively.

① **Connector의 3D Baseline model 생성:** 공진 원인 파악
② **3D Baseline model로 부터 1D distributed TL model 생성:** 공진-> Short stub, TL parameters -> 2D 해석 결과 반영, 기타-> fitting circuit등 추가
③ **1D model로 부터 빠르게 최적화한 결과를 3D 모델에 적용하여 최종 성능 확인 -> 속도 개선**

2. DesignCon 2024 자료 소개

2-9 : Using Fast Multipole Methods to Speed Up S-Parameter Transient Simulation, Raj Raghuram (Aurora System) 외

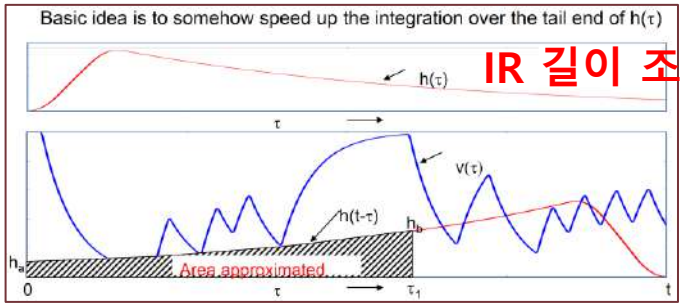
S-parameter를 이용한 Transient 분석의 속도 개선 :

Convolution 장/단점	Vector Fitting
• Find impulse response and most accurate in principle.	• Fit each s-parameter component to a Laplace rational function.
• Slow as we must integrate over whole history of simulation. Gets slower as simulation proceeds.	• Fast once fit is done. Does not get slower as simulation proceeds.
• Causality can be an issue. Passivity usually not a problem.	• Causality guaranteed, but passivity is a problem.
• Initial setup involves finding impulse responses via inverse Fourier Transform. Still doable with hundreds of ports.	• Initial setup involves fitting and passivation. Passivation can take days with 100s of ports.
• Delays modeled well	• Delays not modeled well

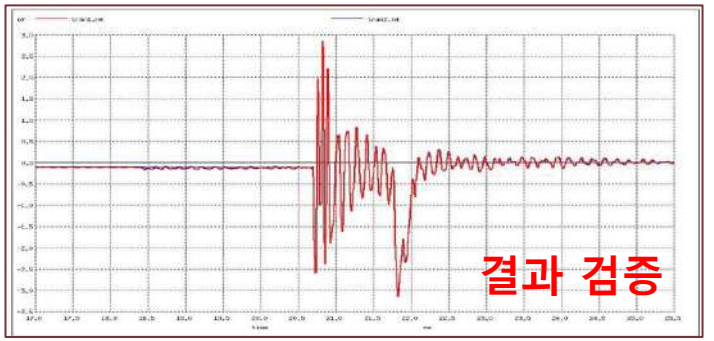
Fast Multipole Method

$$\int_0^{\tau_1} v(\tau)h(t-\tau)d\tau = \int_0^{\tau_1} v(\tau)\sum_{i=1}^{N}\frac{1}{2}A_i\left(e^{j\emptyset_i}e^{\lambda^+_i(t-\tau)} + e^{-j\emptyset_i}e^{\lambda^-_i(t-\tau)}\right)d\tau$$

$$= \sum_{i=1}^{N}\frac{1}{2}A_i\left(e^{j\emptyset_i}e^{\lambda^+_i(t)}\right)\int_0^{\tau_1} v(\tau)e^{\lambda^+_i(-\tau)}\,d\tau + \sum_{i=1}^{N}\frac{1}{2}A_i\left(e^{-j\emptyset_i}e^{\lambda^-_i(t)}\right)\int_0^{\tau_1} v(\tau)e^{\lambda^-_i(-\tau)}\,d\tau$$



IR 길이 조정 방법



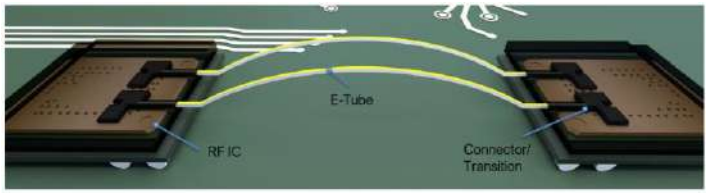
결과 검증

① **Convolution 방식의 단점: 적분 연산 속도**
② **Impulse response 길이 조절 접근:**
Application에 따른 정확도 vs 속도 trade off
③ **Fast Multipole Method를 이용하여 적분 연산 복잡도 개선:**
Convolution 대신 1회 적분 -> 재사용, O(n^2)-> O(nlog(n))

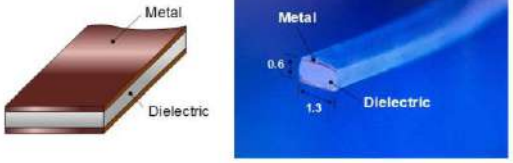
2. DesignCon 2024 자료 소개

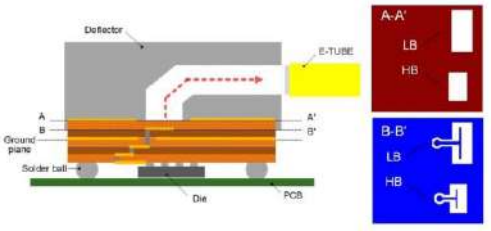
2-10 : E-Tube : RF Plastic Dielectric Waveguide for Terabit High-Speed Interconnect , Ha-IlSong(Point2 Technology) 외

- E-tube는 AI/ML 데이터 센터 구축에 필요한 장비 연결의 새로운 방법으로 기존 구리나 광 연결 방식대비 성능, 비용, 전력 측면에서 우수한 저가, 저전력의 플라스틱 도파관 솔루션
- 주파수에 독립적인 삽입손실과 그룹지연 특성이 장점
- PCB 패턴에서 도파관 연결부는 광대역 매칭이 가능함
- 3m 2x 112Gbps 듀얼밴드 데이터 통신을 시뮬레이션 평가결과 BER<10e-10를 만족함

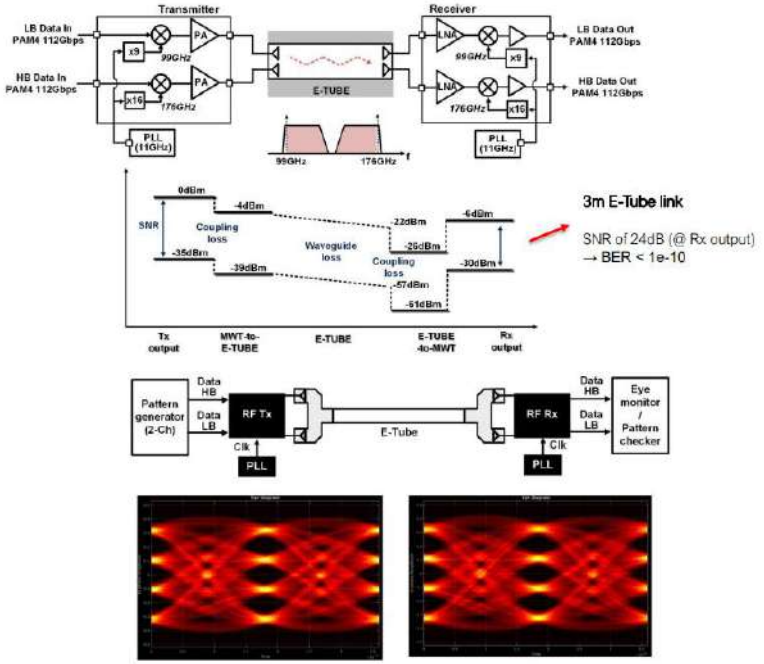


- No skin effect – low channel loss for high data rate signaling
- Plastic straw, No optics - very low cost
- Vertical coupling, Small footprint – high port density





- Dielectric core laminated with thin copper film
  - Core with the metal cladding at the top and the bottom (frequency-independent group delay)
  - Frequency-independent loss of 6dB/m and group delay of 4ns/m
- Chip-to-E-Tube interface
  - RF T/Rx (bottom), LB/HB Microstrip-to-Waveguide Transition (top) and ground plane (middle)
  - Slot-coupled Microstrip-to-Waveguide Transition

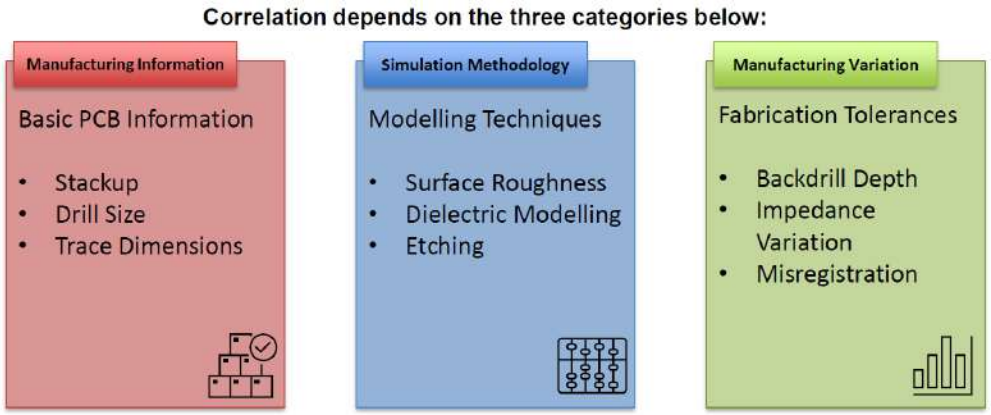


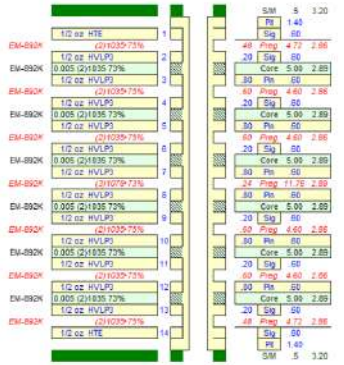
- Eye diagram (PAM4 112Gbps w/ PRBS15)
  - LB output (left), HB output (right)
  - BER of less than 10^{-10} is estimated from the eye diagram results

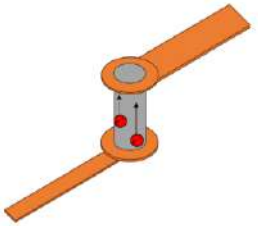
2. DesignCon 2024 자료 소개

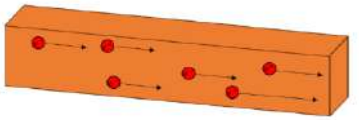
2-11 : Survey on Correlation & Simulation Methodologies for PCB Structures Through 67GHz , Robert Branson (Samtec)

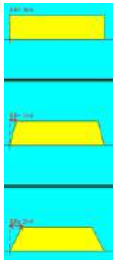
- 정확한 PCB 해석에 필요한 주요 인자를 파악하고 이를 반영한 해석결과는 측정결과와의 차이로 나타나며, 물성 고려 사항은 아래와 같음
- Surface Roughness: PCB 도체의 높이 편차를 나타내며 Dk/Df 또는 Huray 모델 사용
- Dielectric Modelling: 유전체 정보를 나타내며 상수, 레이어별 정보, 제조사 정보 등을 사용
- Conductivity: PCB는 순수 구리보다 낮은 conductivity를 갖음
- Via conductivity: 아직 많은 연구가 이루어지지 않았고 표준이 없음
- Etching: PCB 제조사에 따라 결정되며 임피던스 편차가 발생함
- Copper utilization: 각 레이어의 도체 비율에 따라 prepreg 유전체 높이 조정





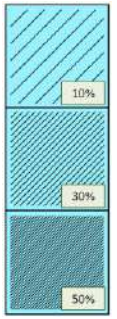






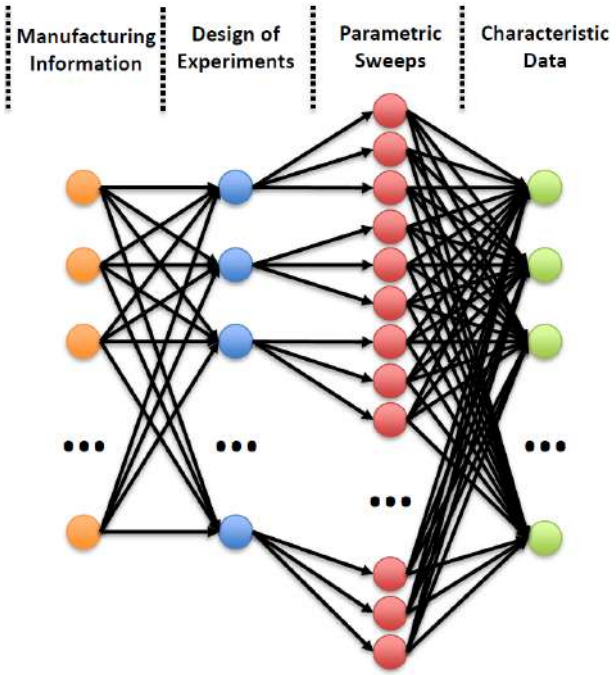
$$EF = \frac{2 * Thickness}{TW_{Bottom} - TW_{Top}}$$

$$Thickness = Nominal\ Thickness - Foil\ Thickness * \left(1 - \frac{Copper\ Utilization\ \%}{100}\right)$$



2-11 : Survey on Correlation & Simulation Methodologies for PCB Structures Through 67GHz , Robert Branson (Samtec)

- 환경적 요인은 아래와 같음
- Copper temperature: 온도에 따라 계산됨
- Dielectric temperature: 온도는 유전체 손실에 영향이 크지만 아직 연구가 필요함
- Humidity: 습도는 유전율과 유전체 손실에 영향이 크지만, 정확한 측정이 어려움
- Lifespan: 시간과 온도 변화에 따라 도체는 점점 손상되고 유전체는 특성이 나빠짐



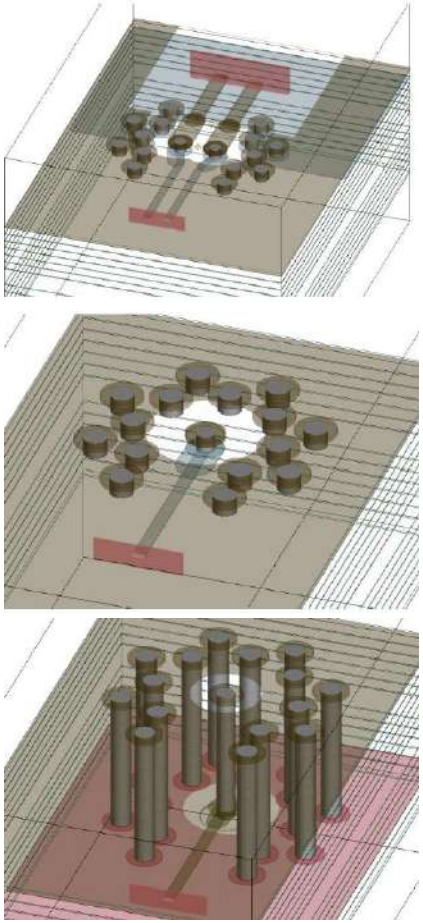
DOE(Design of Experiment) of characteristics

DOE 분석에 사용된 인자들은 슬라이드 뒷부분(Backup) 항목에 표기되어 있습니다. 내용이 많아 요약에는 생략합니다.

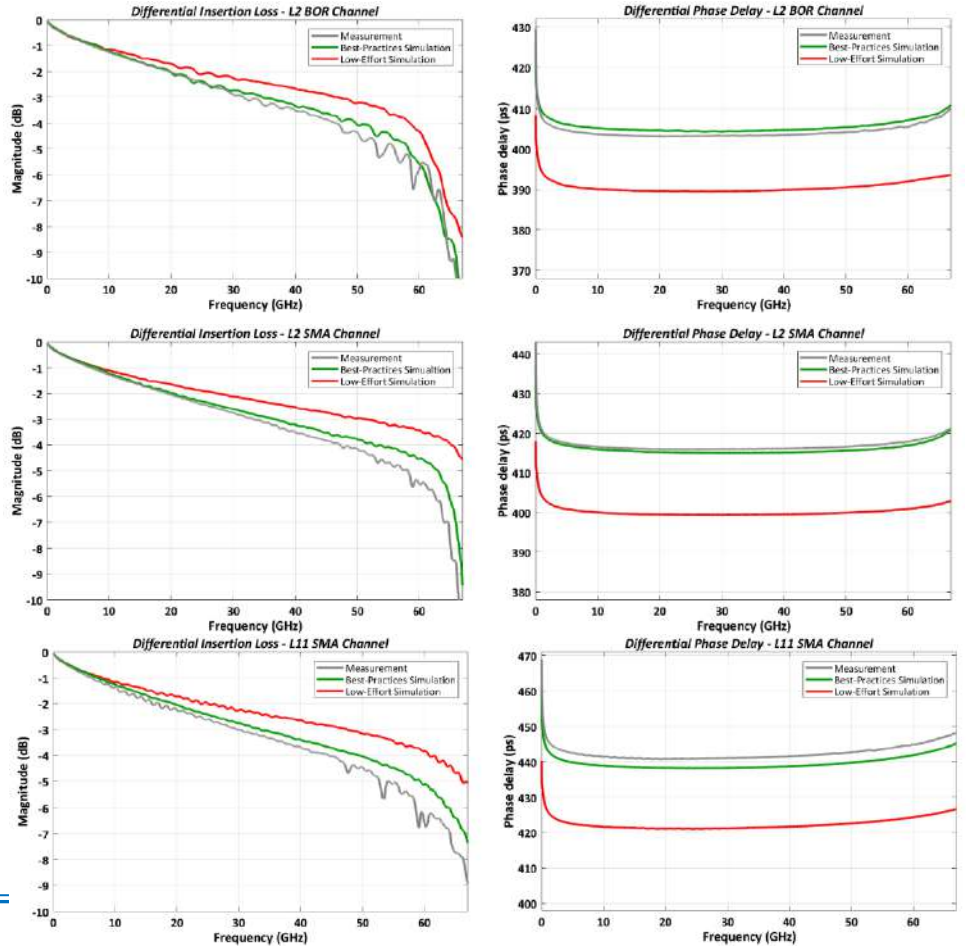
2. DesignCon 2024 자료 소개

2-11 : Survey on Correlation & Simulation Methodologies for PCB Structures Through 67GHz , Robert Branson (Samtec)

- 각 모델링 요소에 따른 해석과 측정 결과 차이



Characteristic	Best-Practices	Low-Effort
Surface Roughness	Modified High-Frequency Huray	Groiss
Dielectric Modelling	Layer-by-Layer with Multiplier on Manufacturer Information	Layer-by-Layer with Manufacturer Information
Conductivity	Characterized Copper Foil	Pure Copper
Via Conductivity	Characterized Via	Pure Copper
Etching	Implemented	Not Implemented
Copper Utilization	Implemented	Not Implemented



2. DesignCon 2024 자료 소개

2-12 : A Novel PCB Footprint for Double-Sides press-fit Stacked Optical Module Application , Shuxiang Li, Yuanzhi Xu. (Cisco System Inc.) 외

- CGT라는 새로운 PCB 풋프린트는 삽입손실, 반사손실, 공통/차동 모드변환, 누화를 개선한 팬아웃 방법을 제공함
- P와 N net 사이, 이웃 net 사이에 via를 대칭으로 삽입하여 임피던스 불연속 개선 및 누화 방지 최적화를 수행함
- Double-sides press-fit 구조에서 누화 방지에 효과적인 방법

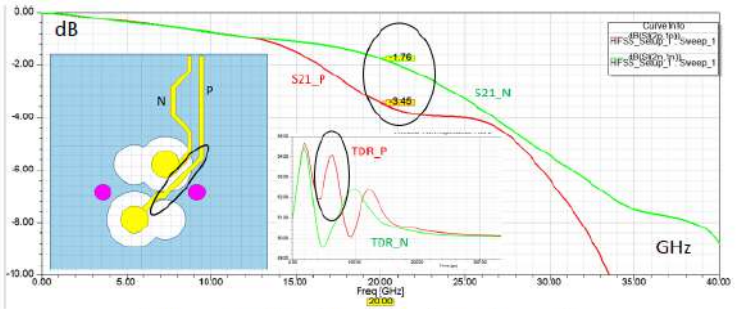


Figure 2-7, Positive lane with broken reference plane

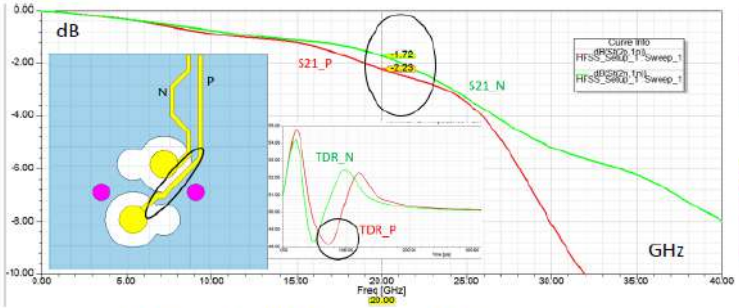
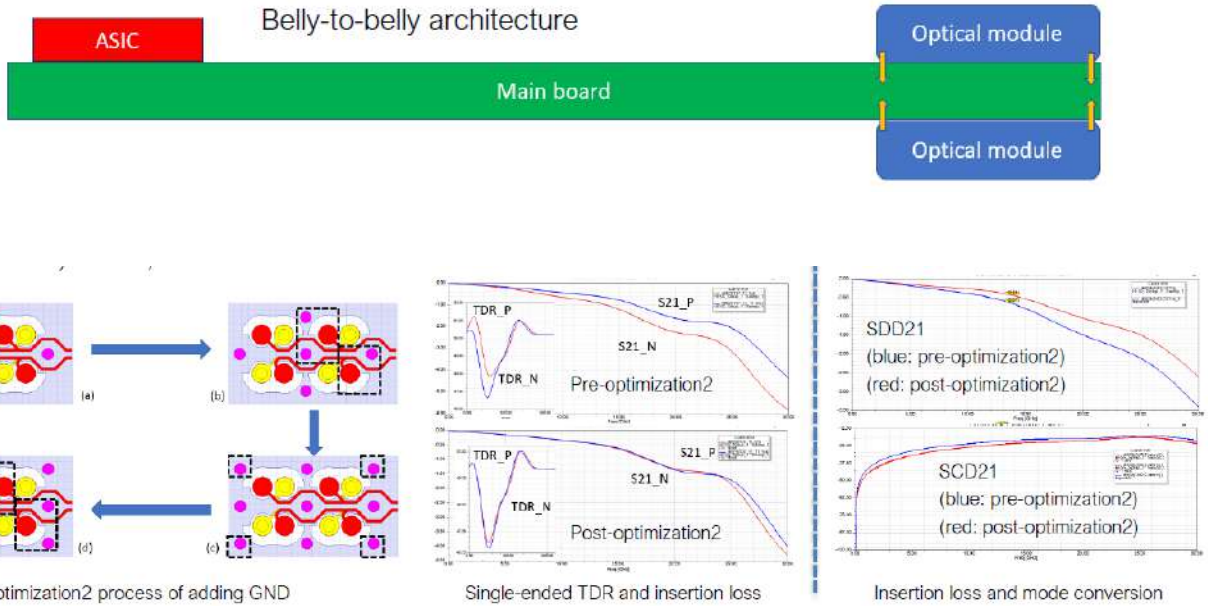


Figure 2-8, Positive lane with integrated reference plane

일반적인 구조의 팬아웃 방법으로 임피던스 불연속에 의한 P/N 불균형 특성을 나타내고 불연속을 수정하여 개선된 결과

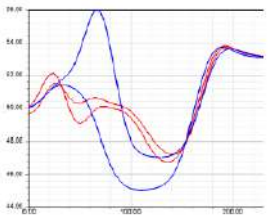


P/N net의 대칭구조의 via를 추가하여 P/N net의 임피던스를 거의 동일하게 최적화하여 SDD21, SCD21 특성을 개선함

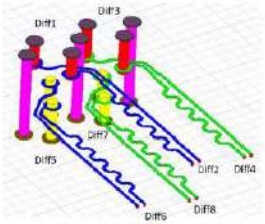
2. DesignCon 2024 자료 소개

2-12 : A Novel PCB Footprint for Double-Sides press-fit Stacked Optical Module Application , Shuxiang Li, Yuanzhi Xu. (Cisco System Inc.) 외

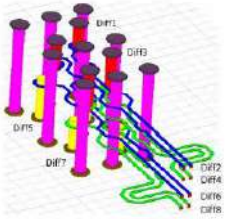
- PCB 측정 결과 모든 특성이 개선됨



Single-ended TDR curves



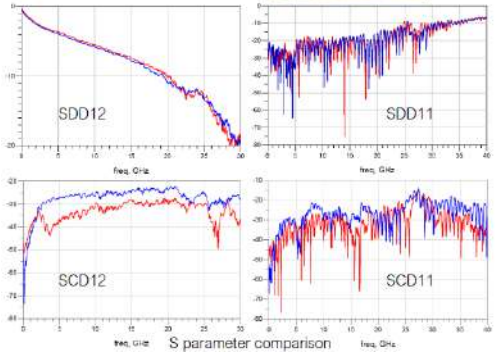
BLUE Conventional model



RED CGT model

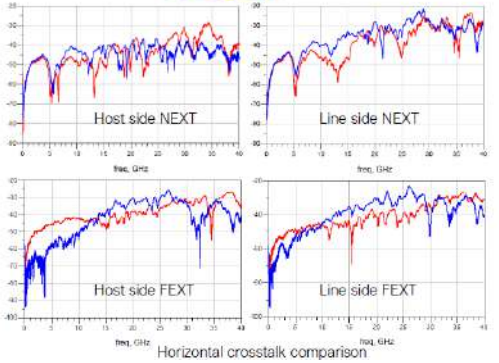
BLUE: Conventional
RED: CGT

Test board



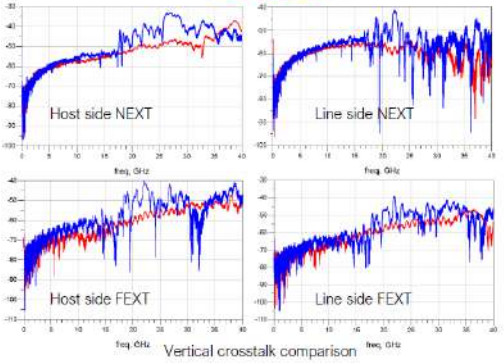
S parameter comparison

One kind of horizontal crosstalk (same row)

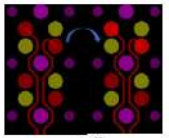


Horizontal crosstalk comparison

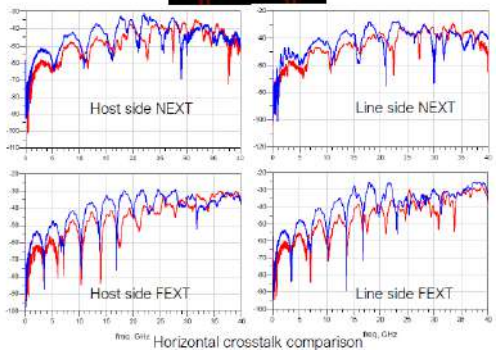
Vertical crosstalk



Vertical crosstalk comparison



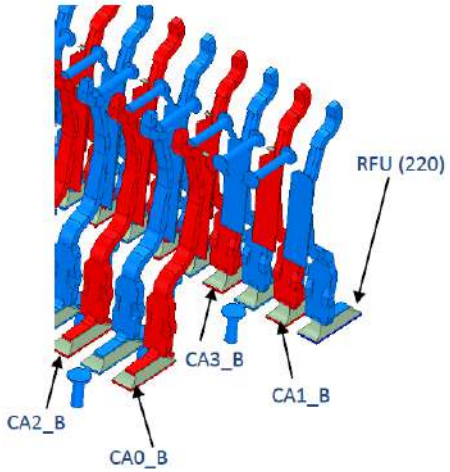
The other kind of horizontal crosstalk (different rows)



Horizontal crosstalk comparison

2-13 : DDR5 System CA Margin Risk and Mitigation , Xiang Li (Intel Corp.)

- Dummy via로 연결된 커넥터 핀 RFU의 영향으로 CA1_B net의 공진이 발생함
- 사용하지 않는 커넥터 핀의 길이를 짧게 수정, 공진주파수를 사용하지 않는 주파수까지 높임
- RFU핀(#220)를 제거하는 표준을 제안함



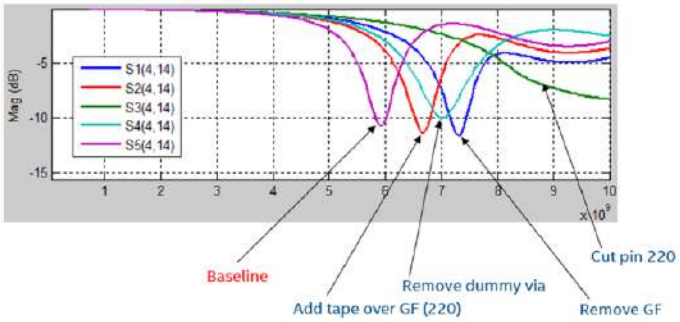
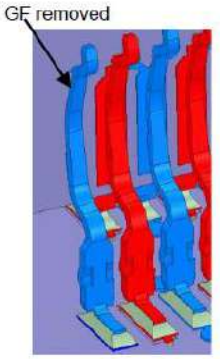
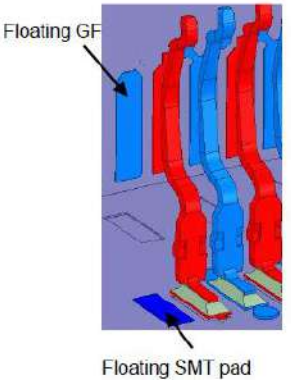
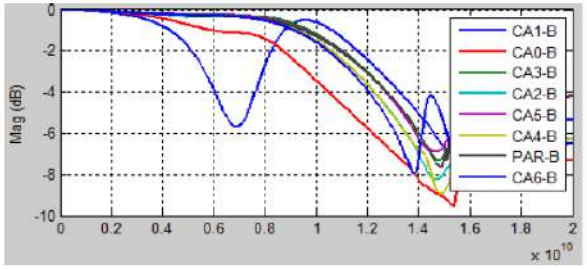


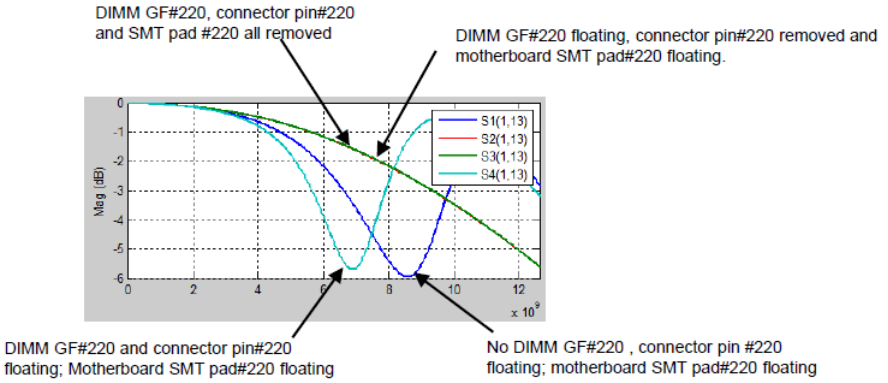
Figure 8. Insertion loss of CA1_B at different rework conditions

플로팅 net의 길이를 짧게 수정할수록 공진주파수는 높아짐





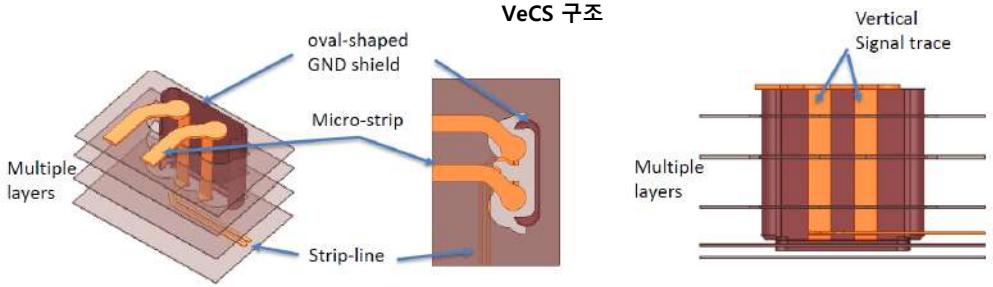




2-14 : Vertical Conductive Structure (VeCS) Technology: Simulation and Measurement , Chaofeng Li, (EMC Lab, M S&T)

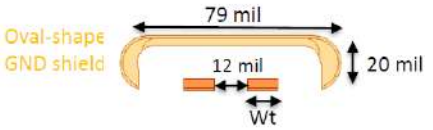
- 기존 구조의 via는 임피던스 불연속, 삽입손실, 누화, 신뢰성, 열 문제를 가지고 있음
- 직사각형 신호 트레이스와 반 동축 타원형의 차폐 접지로 구성하여 손실과 누화 특성 향상됨
- 신호 트레이스 미세 조정이 가능하여 임피던스 최적화가 용이함

VeCS 구조



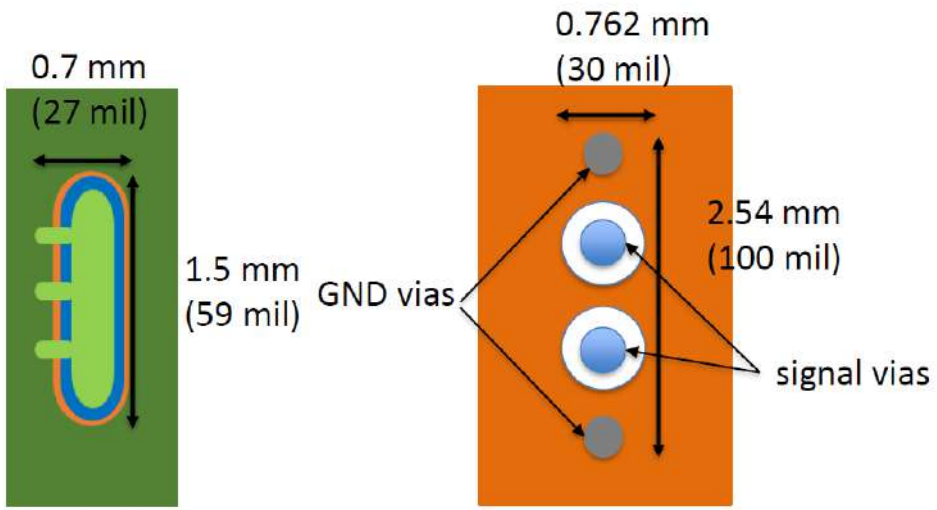
<3D view of VeCS> <Top view of VeCS> <Side view of VeCS>

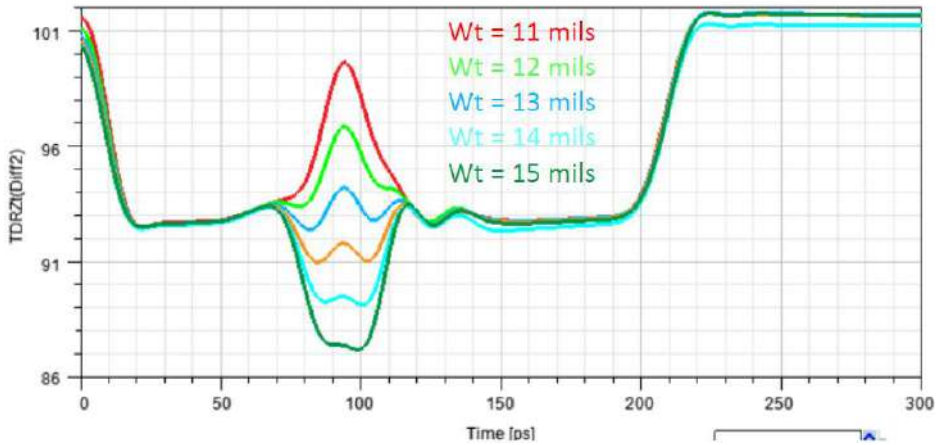
Vertical signal trace length is 73 mils



<Top view of the designed VeCS>

기존 구조 via와 VeCS 레이아웃 면적 비교

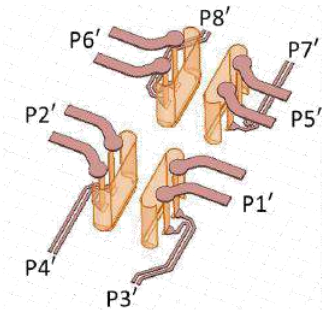




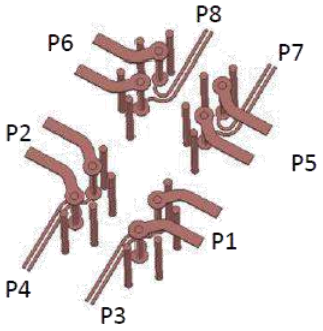
2. DesignCon 2024 자료 소개

2-14 : Vertical Conductive Structure (VeCS) Technology: Simulation and Measurement , Chaofeng Li, (EMC Lab, M S&T)

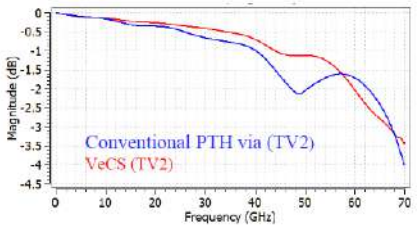
➢ 해석 및 실측 결과 VeCS의 손실과 누화 특성이 우수함

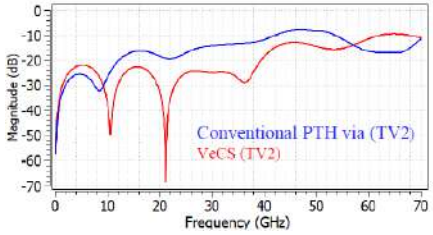


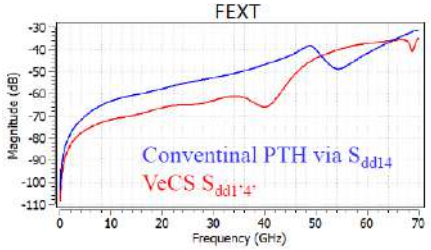
<3D model of VeCS>

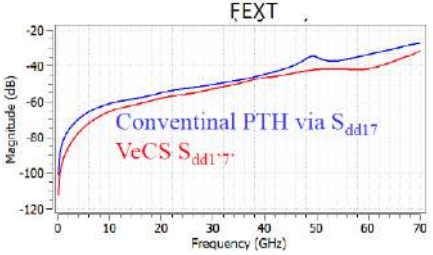


<3D model of conventional via>

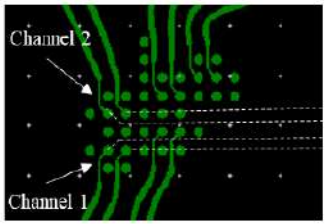


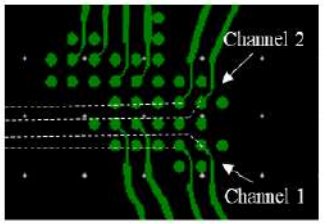


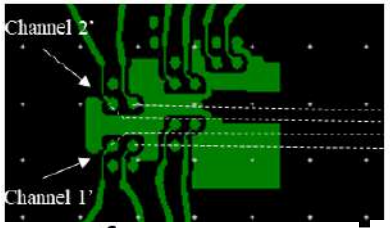


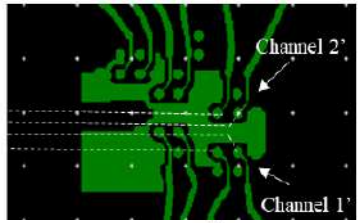


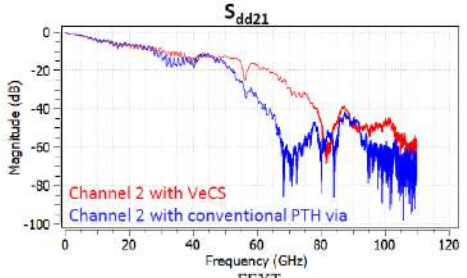
기존 구조 via와 VeCS 해석 결과 비교

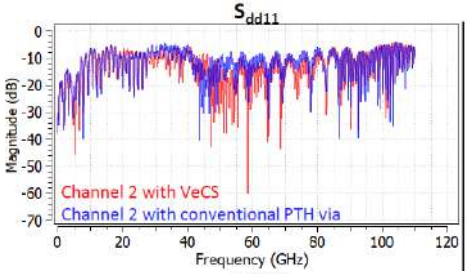


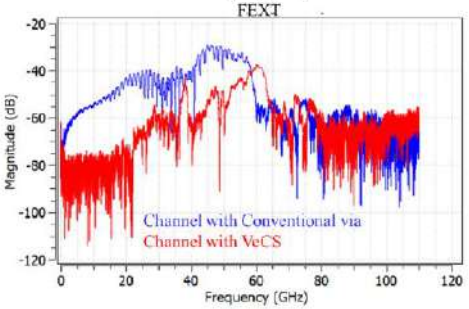


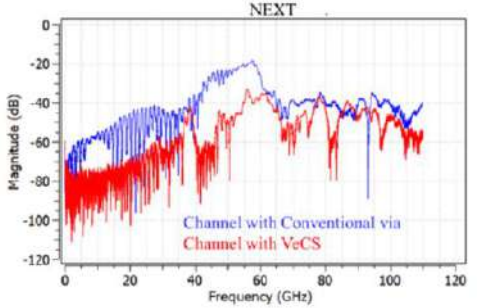












기존 구조 via와 VeCS 측정 결과 비교

Leading the Simulation Market for 50 Years

#1 IN ENGINEERING SIMULATION SOFTWARE

The Industry Leader

Simulation is Our Core Business

Uniquely Positioned for Growth

Setting the Gold Standard for Simulation Solutions

GOLD STANDARD IN EVERY MARKET

Comprehensive Simulation Suite

Simulation Accuracy

Expert Engineering Partner

Open Ecosystem

ANSYS Huwin

Thank You