2026 Semiconductor Simulation Trend

3DL Q3D/HBM/TSV/Microbump

Brandon Kim
Senior Architect

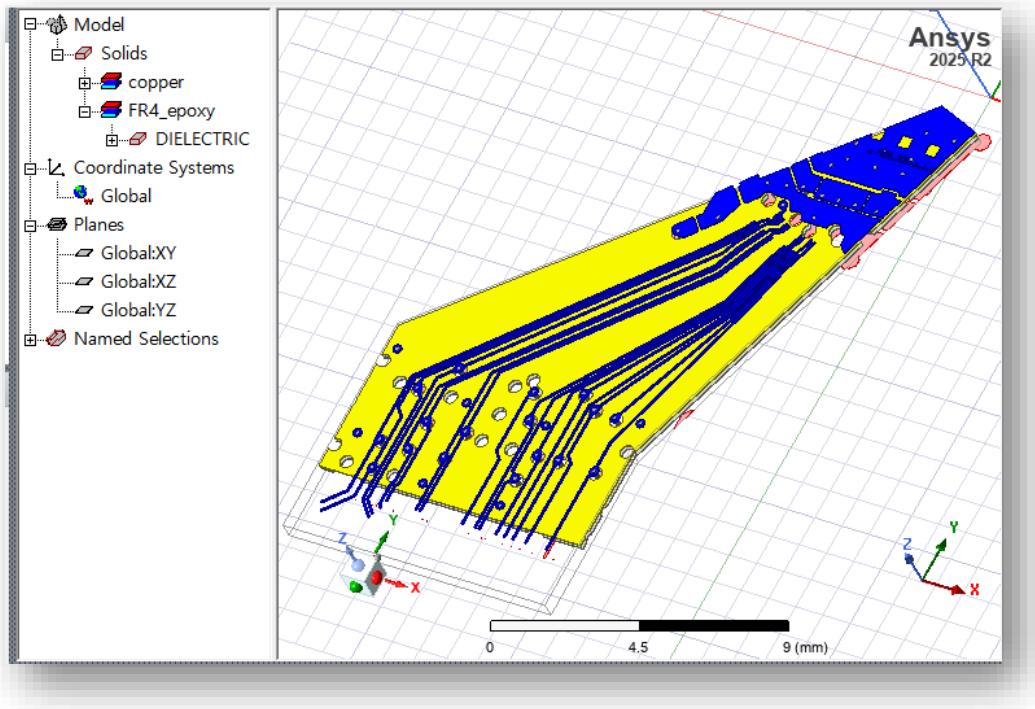
Agenda

- Q3D in 3D Layout : Pros & Cons
- TSV array simulation & automation
- Microbump thermal simulation

Q3D in 3D Layout :

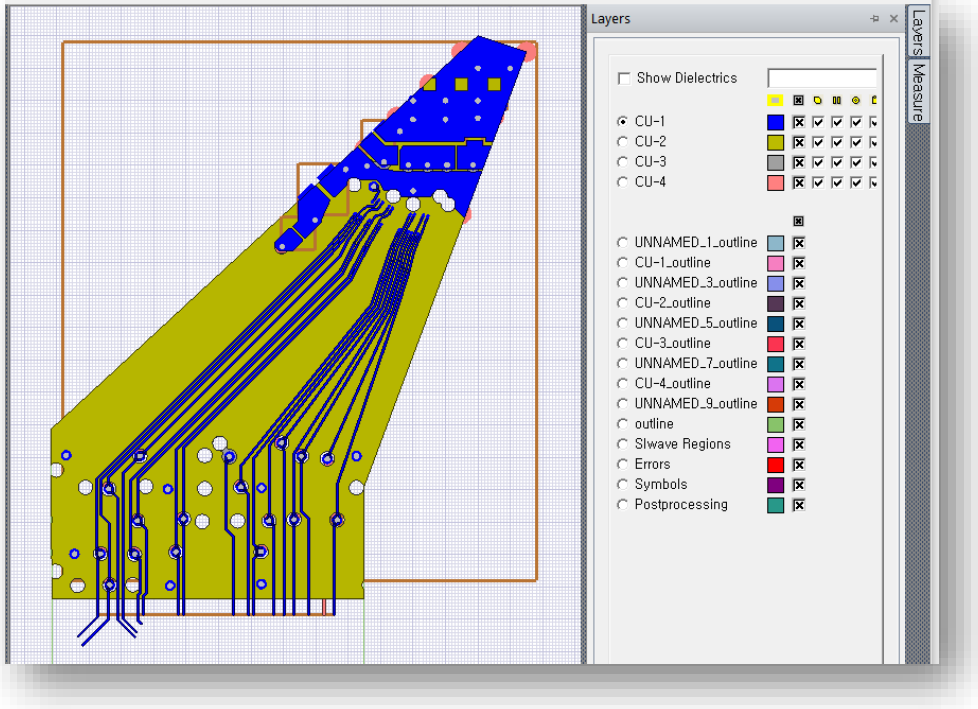
Pros & Cons

MCAD Q3D vs. 3DL Q3D



MCAD Q3D

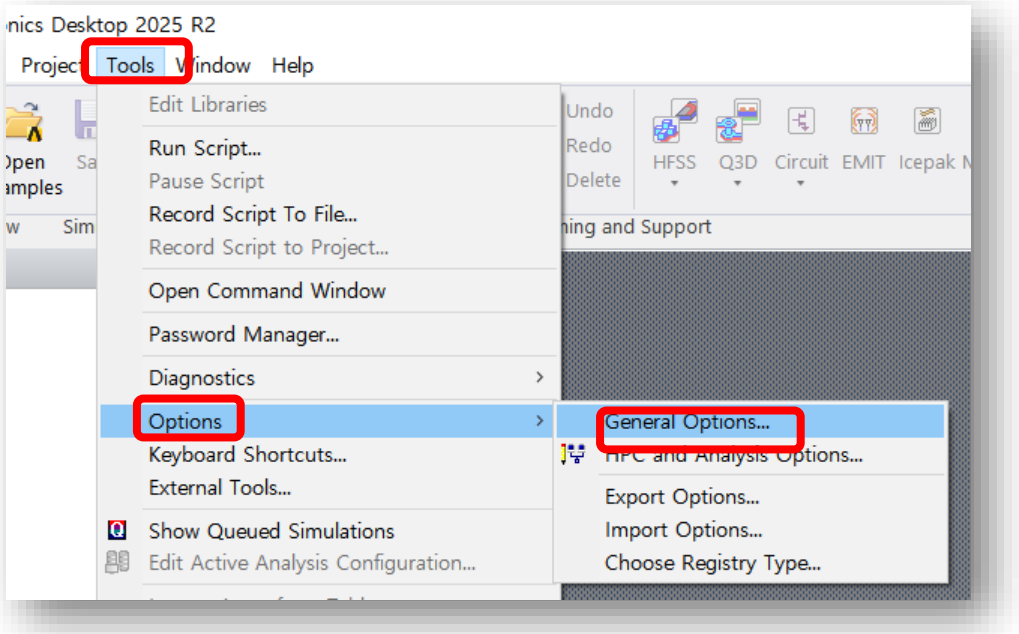
- Conventional Full 3D modeling based on Parasolid 3D modeler

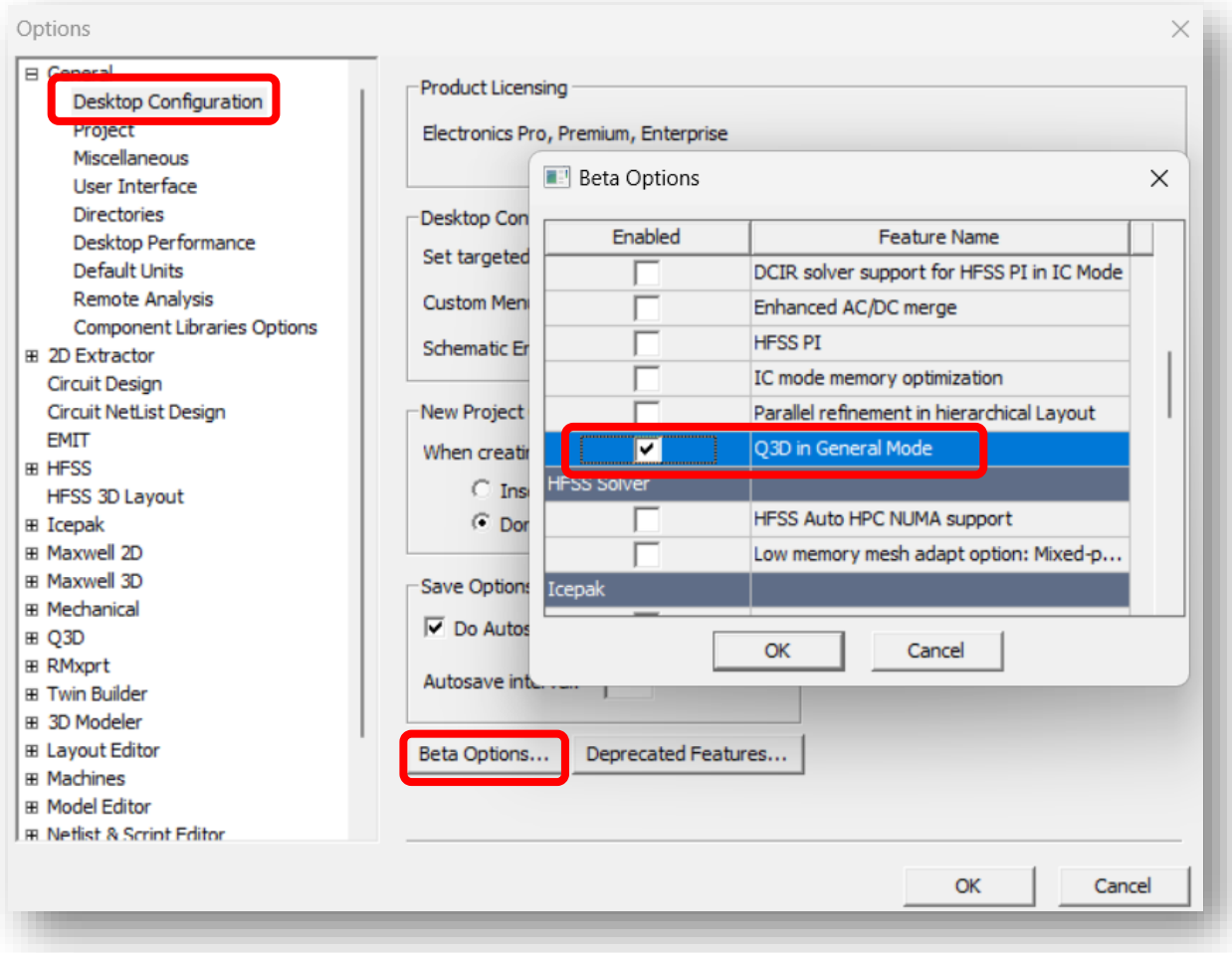


Q3D in 3D Layout

- PCB/PKG only with Net & Layer based on ECAD viewer

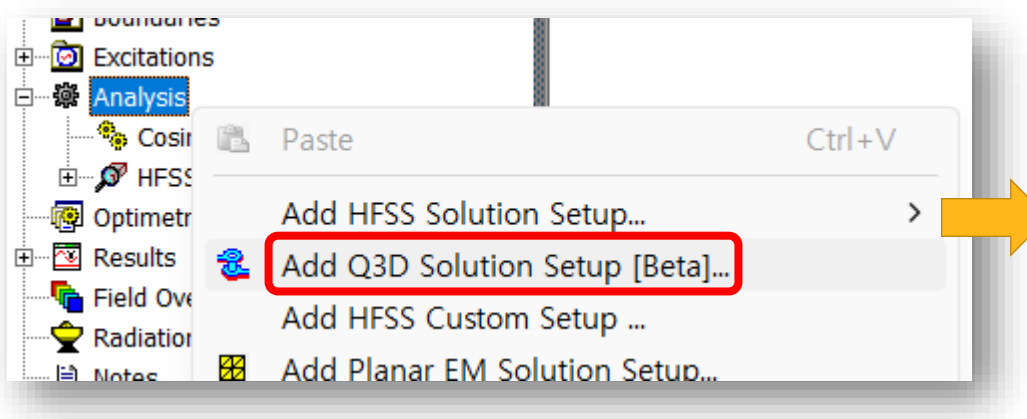
STEP 1 : Q3D in General Mode Setup (Beta)



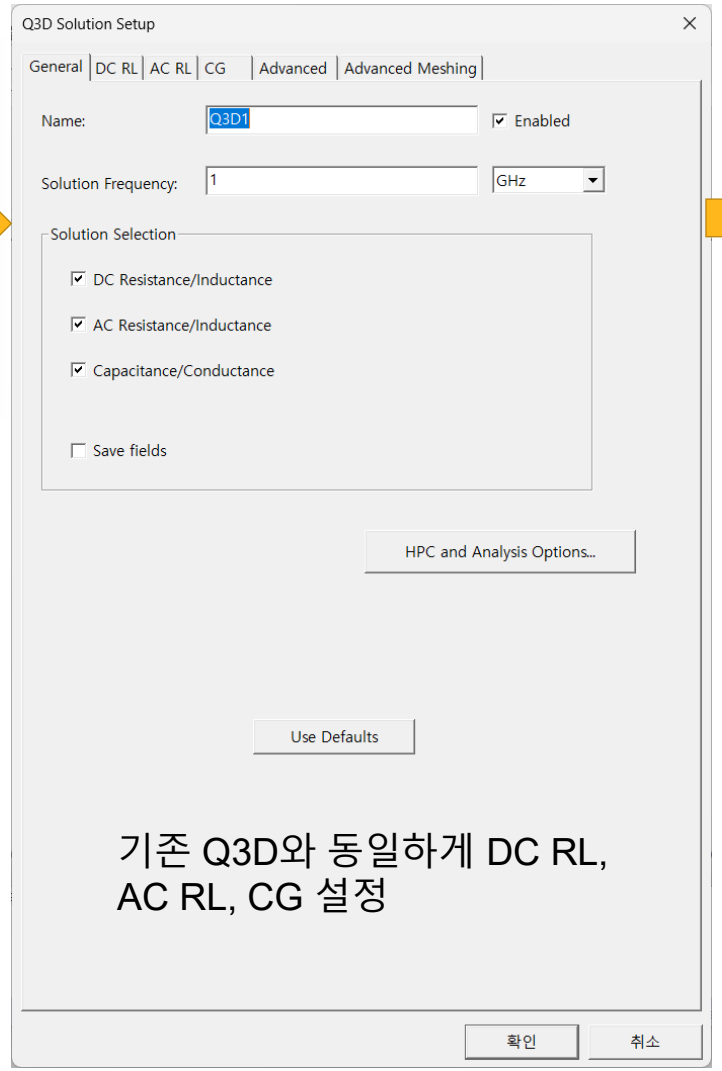


- IC mode에서는 정식 기능
- General mode에서는 Beta 기능으로서, Option에서 활성화시켜야 사용 가능

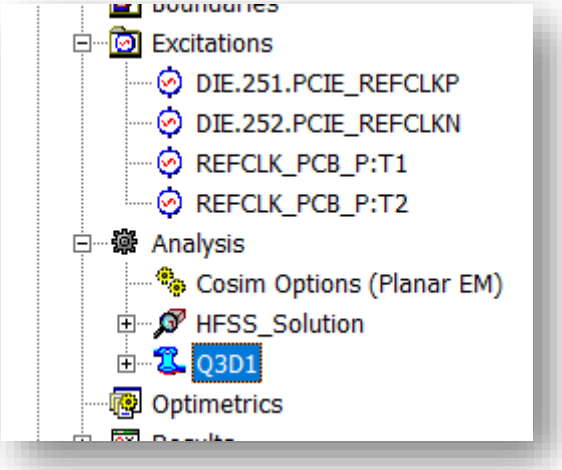
STEP 2 : HFSS 3D Layout - Q3D Setup 추가



Analysis에서 Q3D setup 추가

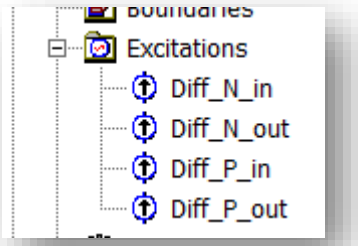


기존 Q3D와 동일하게 DC RL, AC RL, CG 설정

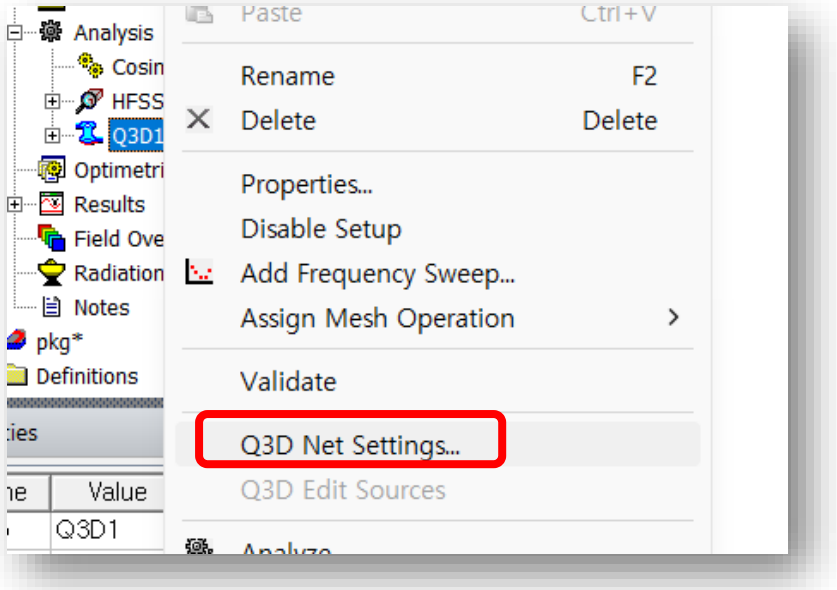


Q3D setup 생성

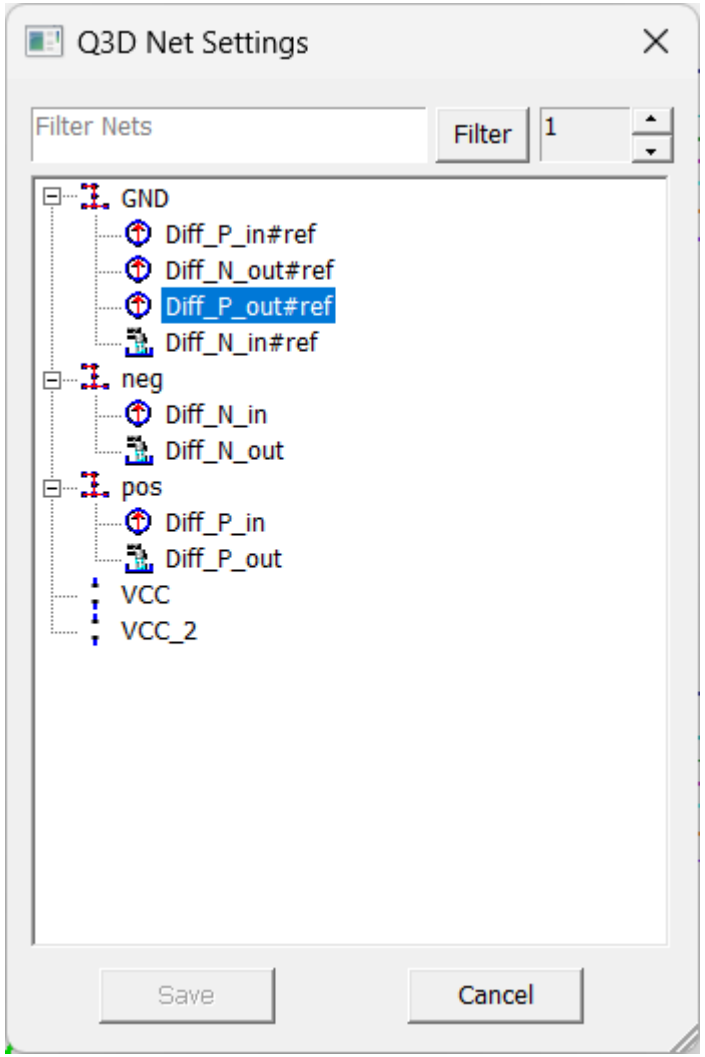
STEP 3 : Q3D net (source/sink) 설정 in HFSS 3D Layout



HFSS Port 설정

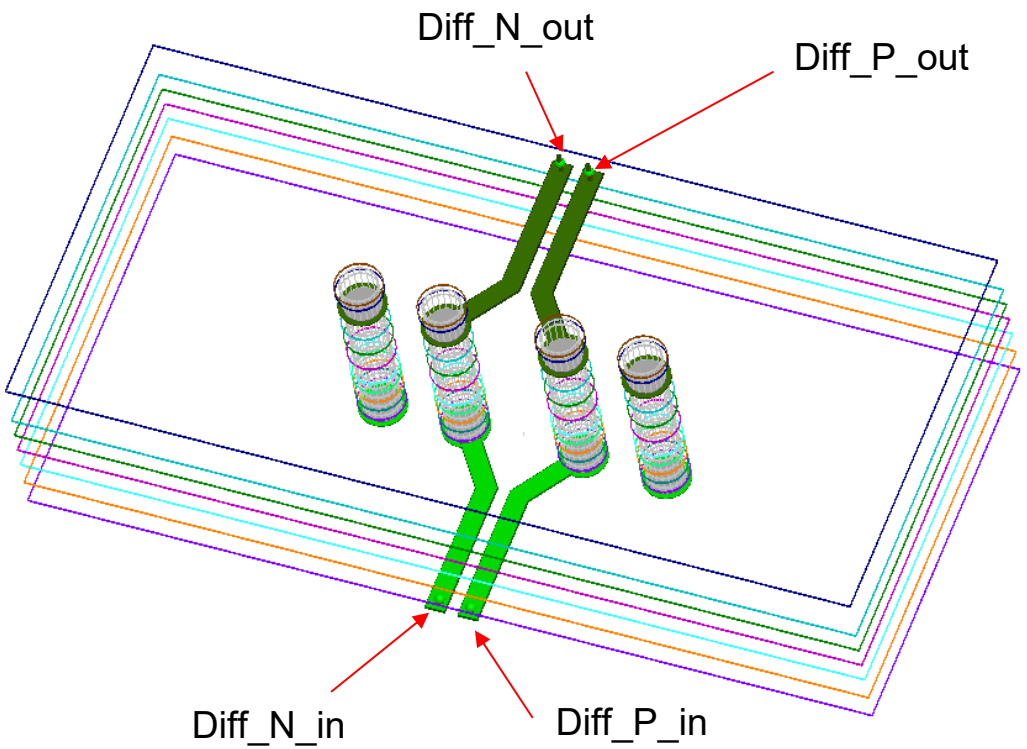


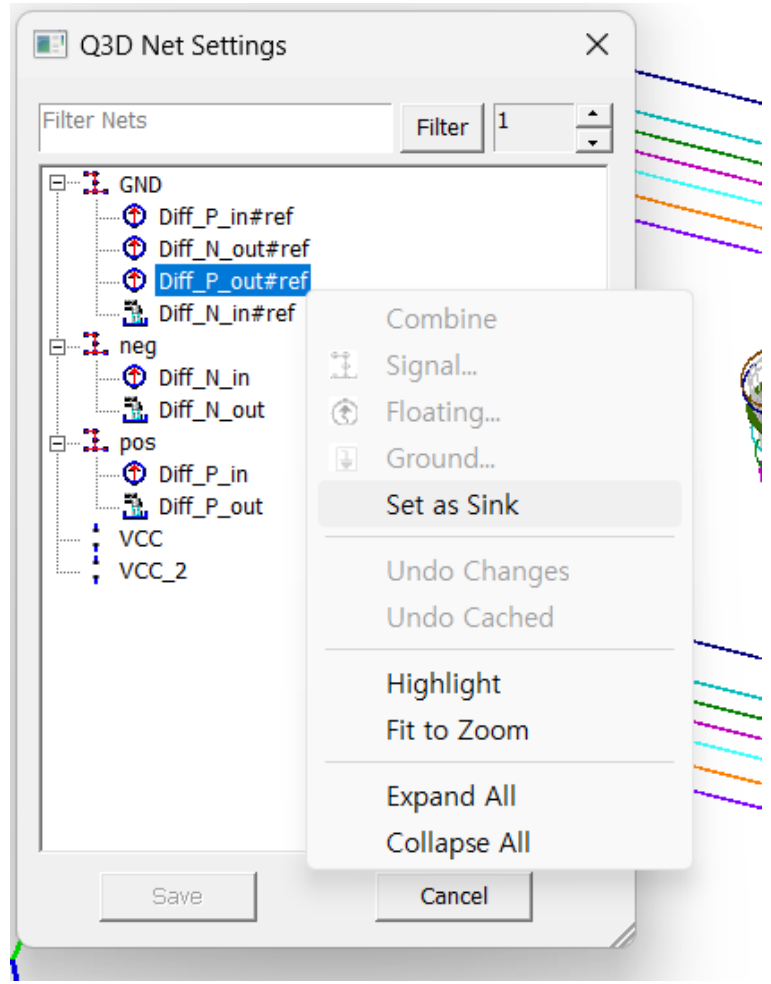
Q3D setup에서 우클릭 →
Q3D Net Seetings



HFSS Port terminal을 기준으로
자동으로 source/sink와 net이 설정됨

STEP 4 : Automatic Source/Sink Assign & modifying

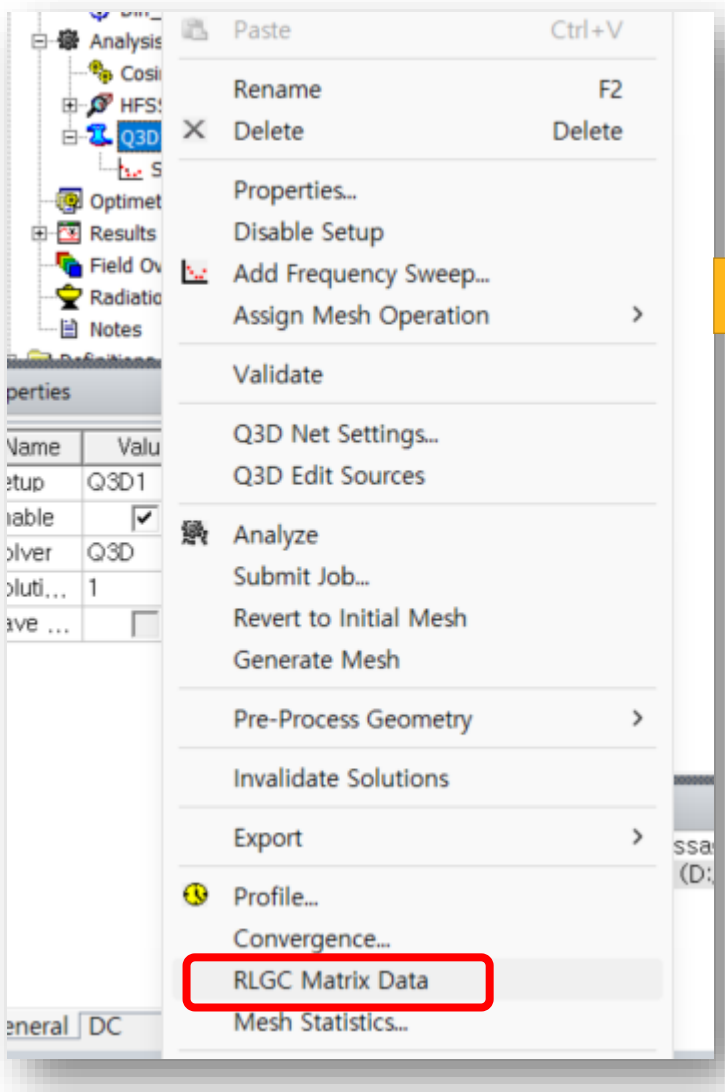


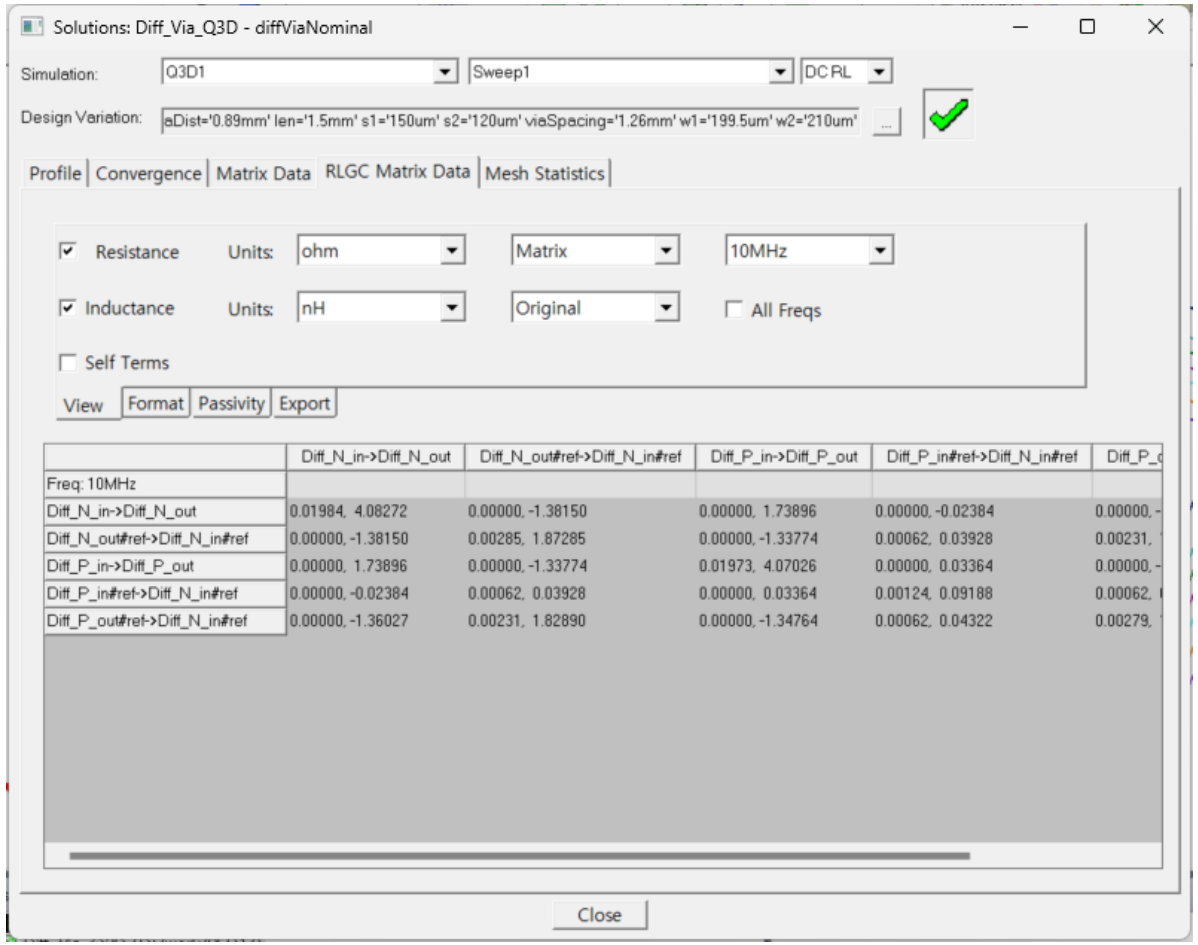


미리 생성된 HFSS Port 를 기준으로
→ Signal net 시작과 끝에 자동으로 source/sink 배치
→ 공통 Reference net에 1개의 sink와 나머지는 source 자동 배정
- Wave port는 불가능, terminal과 lumped port만 가능

User가 source/sink를 변경 가능

STEP 5 : RLGC Result





	Diff_N_in->Diff_N_out	Diff_N_out#ref->Diff_N_in#ref	Diff_P_in->Diff_P_out	Diff_P_in#ref->Diff_N_in#ref
Freq: 10MHz				
Diff_N_in->Diff_N_out	0.01984, 4.08272	0.00000, -1.38150	0.00000, 1.73896	0.00000, -0.02384
Diff_N_out#ref->Diff_N_in#ref	0.00000, -1.38150	0.00285, 1.87285	0.00000, -1.33774	0.00062, 0.03928
Diff_P_in->Diff_P_out	0.00000, 1.73896	0.00000, -1.33774	0.01973, 4.07026	0.00000, 0.03364
Diff_P_in#ref->Diff_N_in#ref	0.00000, -0.02384	0.00062, 0.03928	0.00000, 0.03364	0.00124, 0.09188
Diff_P_out#ref->Diff_N_in#ref	0.00000, -1.36027	0.00231, 1.82890	0.00000, -1.34764	0.00062, 0.04322

- RLGC 결과를 확인하는 방법은 기존 Q3D와 동일

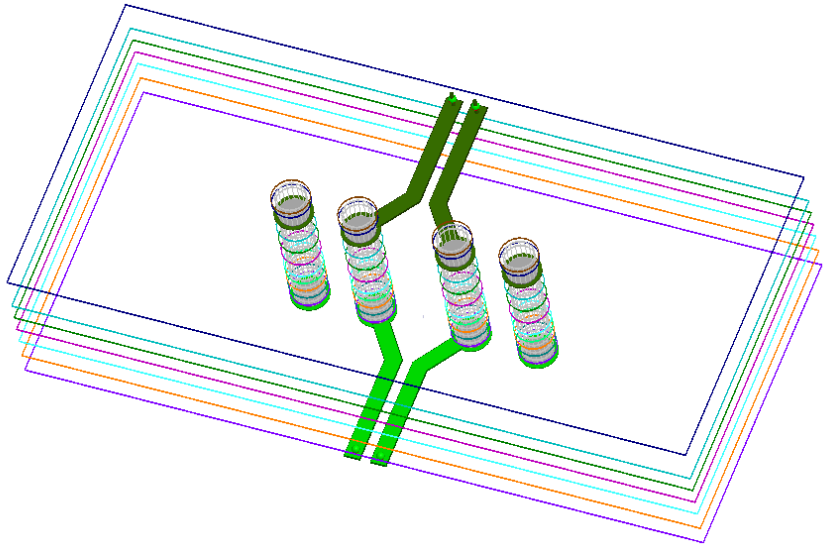
Q3D in HFSS 3D Layout 의 장점

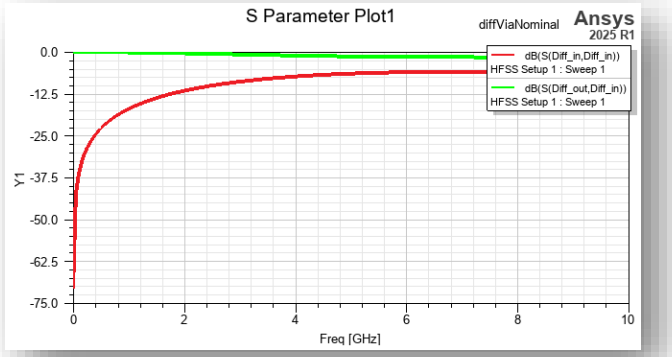
1. HFSS 를 위한 모델과 셋업 그대로 즉시 Q3D solver를 돌릴 수 있음
   - 별도로 Q3D export 및 source/sink modeling이 필요 없음

2. HFSS 3D Layout 특유의 빠르고 가벼운 GUI를 활용할 수 있음
   - 복잡하고 큰 모델의 경우, 기존의 Q3D보다 작업효율이 크게 개선됨

3. Intersection check와 Finding Net 과정이 생략되어 해석속도 증가

→ 동일한 모델로 한꺼번에 HFSS S parameter와 Q3D RLGC 데이터를 추출 가능





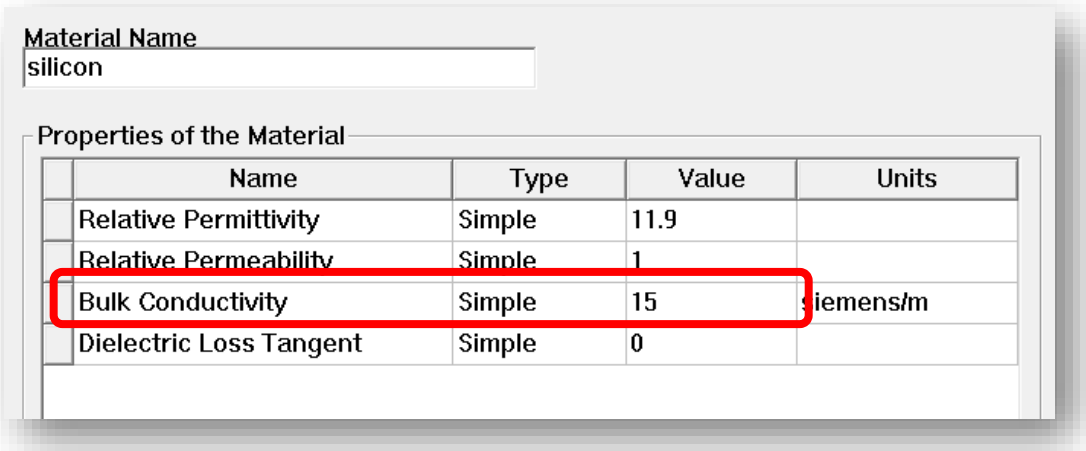
	Diff_N_in->Diff_N_out	Diff_N_out#ref->Diff_N_in#ref	Diff_P_in->Diff_P_out	Diff_P_in#ref->Diff_N_in#ref	Diff_P_out#ref->Diff_N_in#ref
Freq: 10MHz					
Diff_N_in->Diff_N_out	0.01984, 4.08272	0.00000, -1.38150	0.00000, 1.73896	0.00000, -0.02384	0.00000, -1.36027
Diff_N_out#ref->Diff_N_in#ref	0.00000, -1.38150	0.00285, 1.87285	0.00000, -1.33774	0.00062, 0.03928	0.00231, 1.82890
Diff_P_in->Diff_P_out	0.00000, 1.73896	0.00000, -1.33774	0.01973, 4.07026	0.00000, 0.03364	0.00000, -1.34764
Diff_P_in#ref->Diff_N_in#ref	0.00000, -0.02384	0.00062, 0.03928	0.00000, 0.03364	0.00124, 0.09188	0.00062, 0.04322
Diff_P_out#ref->Diff_N_in#ref	0.00000, -1.36027	0.00231, 1.82890	0.00000, -1.34764	0.00062, 0.04322	0.00279, 1.86597

MCAD Q3D vs. 3DL Q3D : Detail Comparison

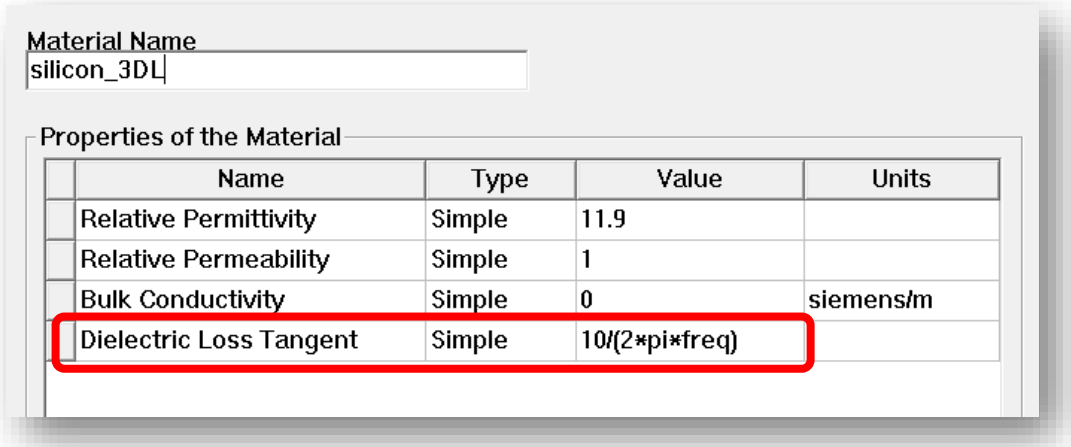
	MCAD Q3D	3DL Q3D	3DL Workaround
Result/Terminal	RLC extraction only based on 2D source/sink	**RLC extraction & HFSS/SIwave sim based on port**	
GUI rendering	Slow (Full 3D)	**Super-fast** (ECAD)	
Intersection check	Yes (can be minimized)	**No need**	
Finding net process	Yes (can be ignored)	**No need**	
tanδ + Conductivity Setup	Possible	**No**	tanδ compensation
Automation script	100% support	**80% support**	Hard coding
Accuracy	Golden Standard	To be correlated	
Simulation Speed		**About 10~50% faster**	

Silicon is semiconductor..

MCAD Q3D



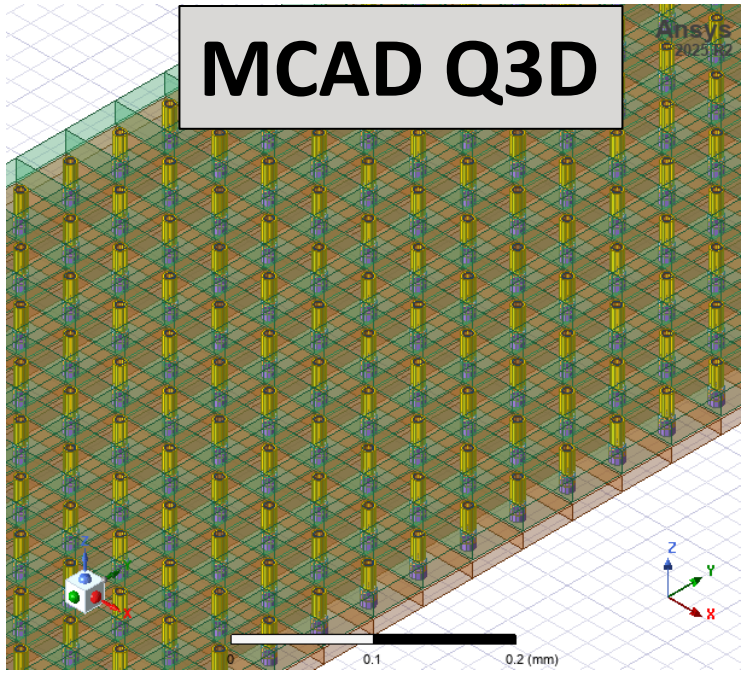
3DL Q3D

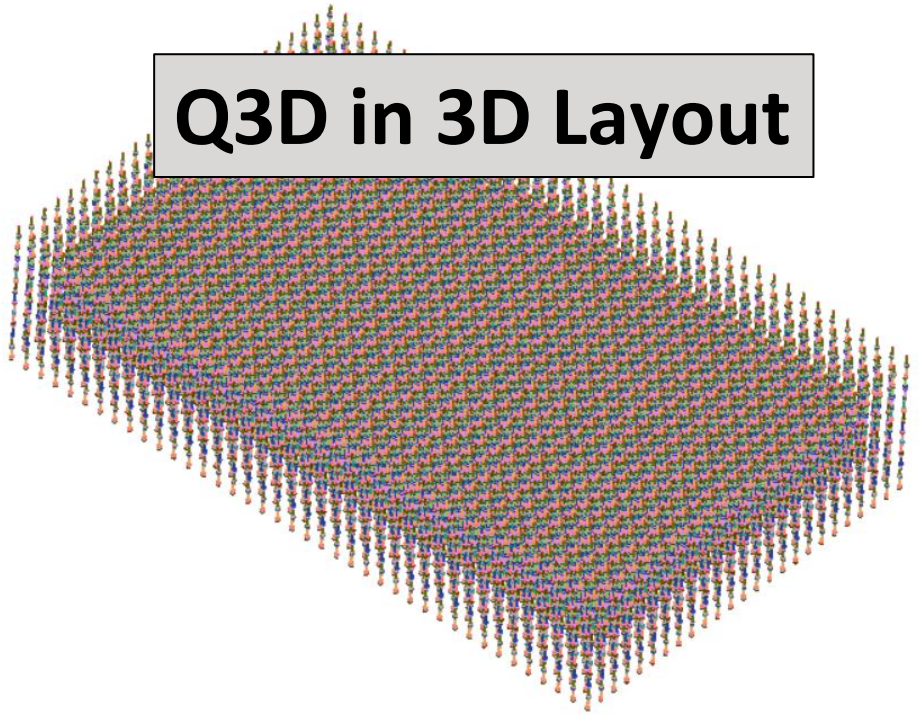


$$\varepsilon\_eff = \varepsilon' - j(\varepsilon' \cdot \tan\delta + \sigma/\omega)$$

- User can set Dielectric property and conductivity at the same time in MCAD Q3D
- Conductivity works as a loss term and effects to G(Transconductance) value
- User can set loss tangent with conductivity in the 3DL Q3D

Key Summary : MCAD Q3D vs. 3DL Q3D

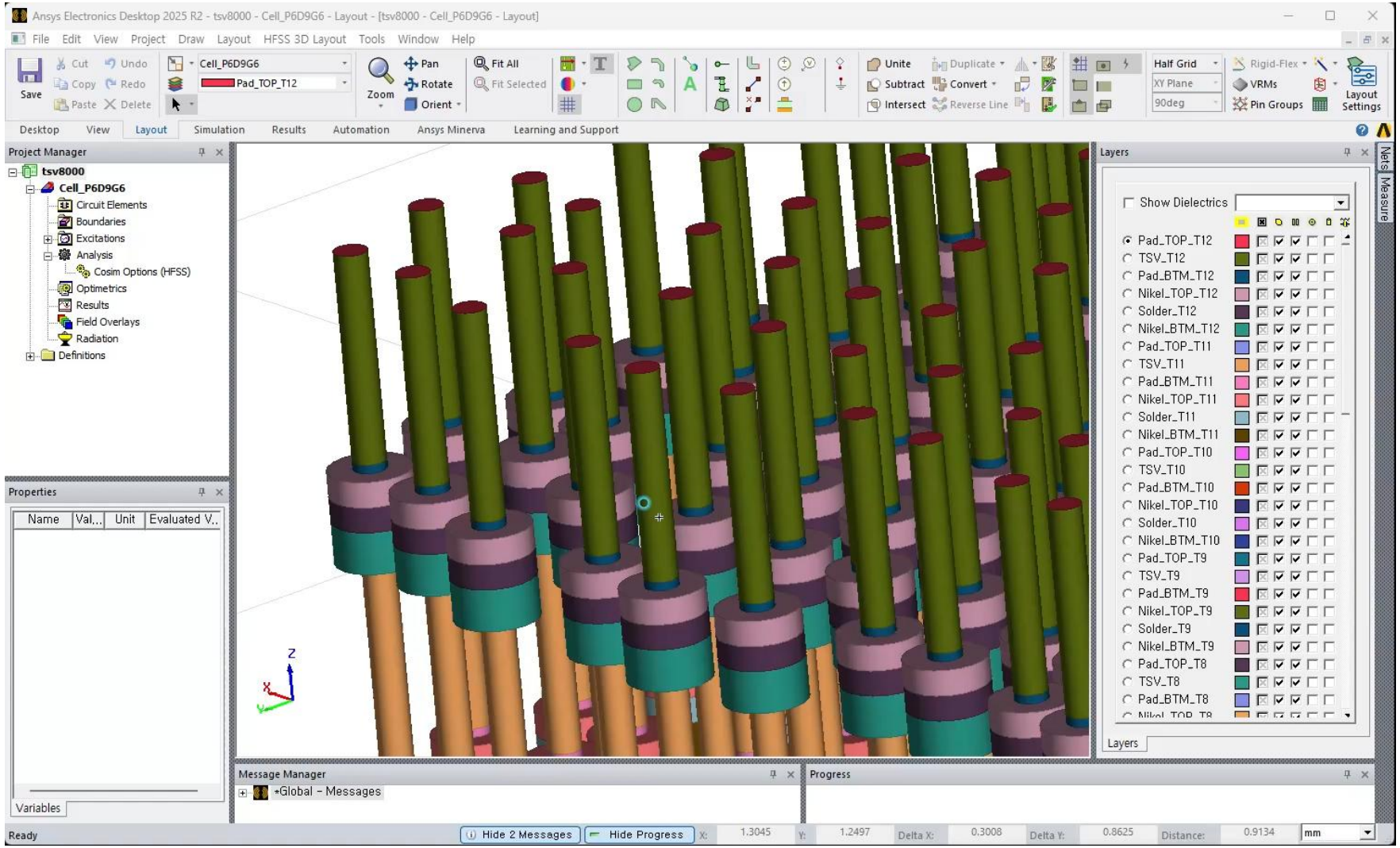




- Golden Standard
- Set loss tangent + conductivity : possible
- Stable automation (IPY script, PyAEDT)
- Long finding net / intersection check time
- Slow GUI rendering

- To be correlated to MCAD Q3D result
- Set loss tangent + conductivity : Work around
- beta automation (PyEDB) : Work around
- No finding net / intersection check
- Super fast GUI rendering

3DL Q3D : Super-fast GUI



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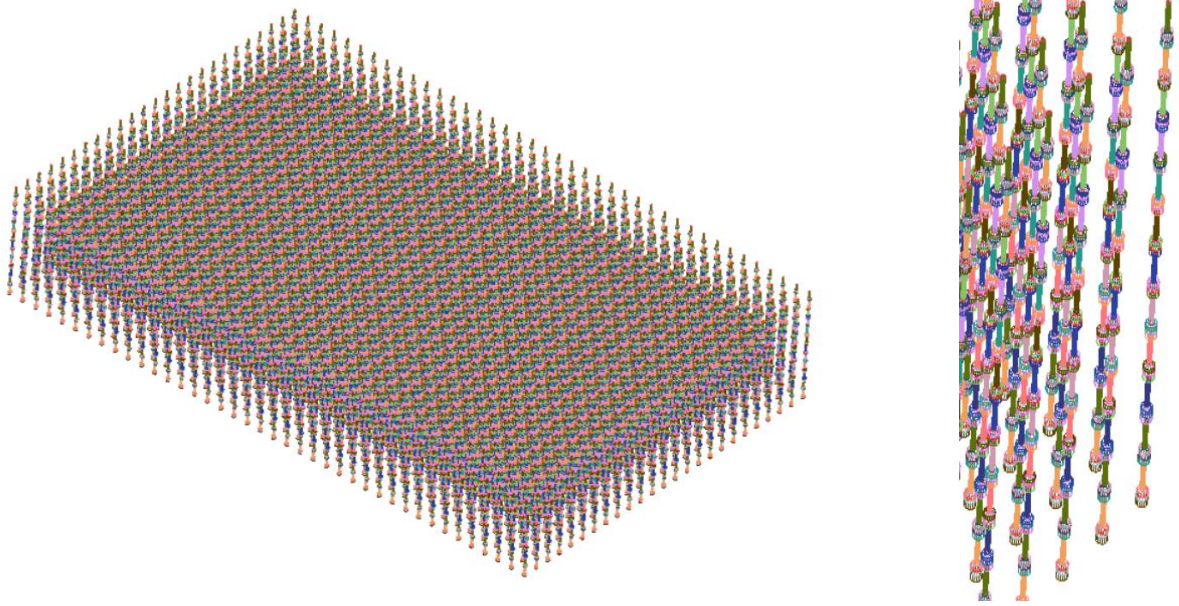
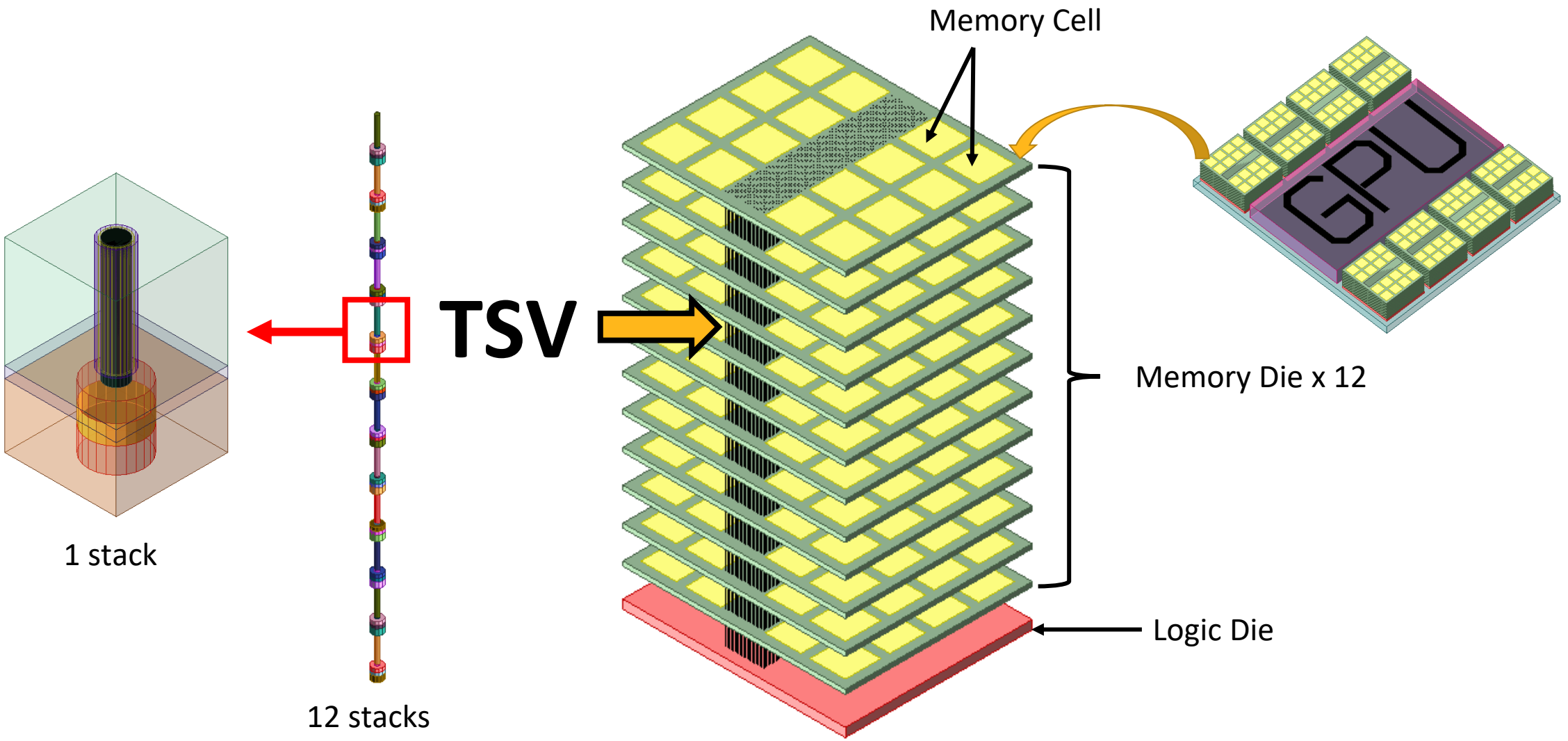
HBM TSV array simulation



TSV in HBM4



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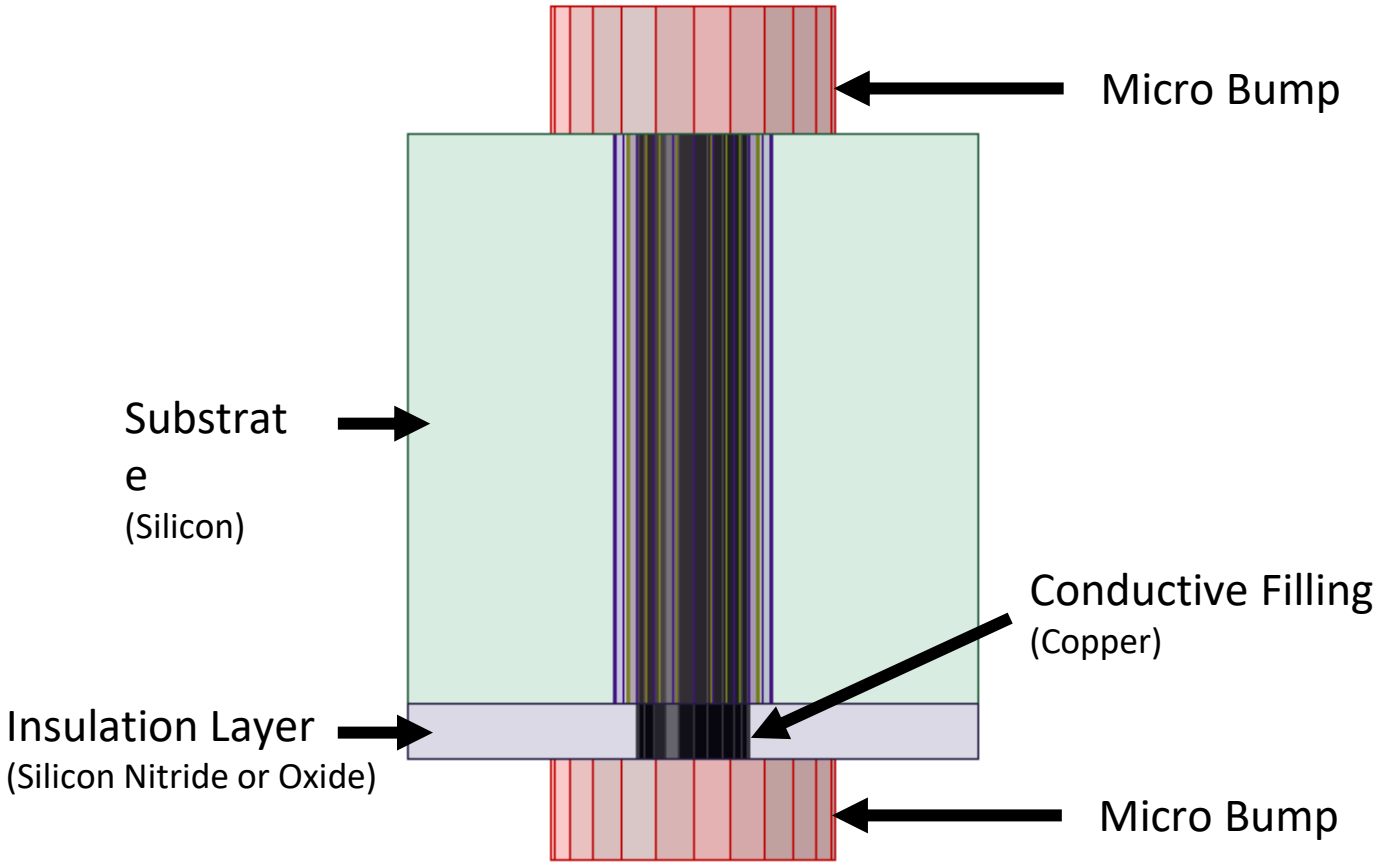
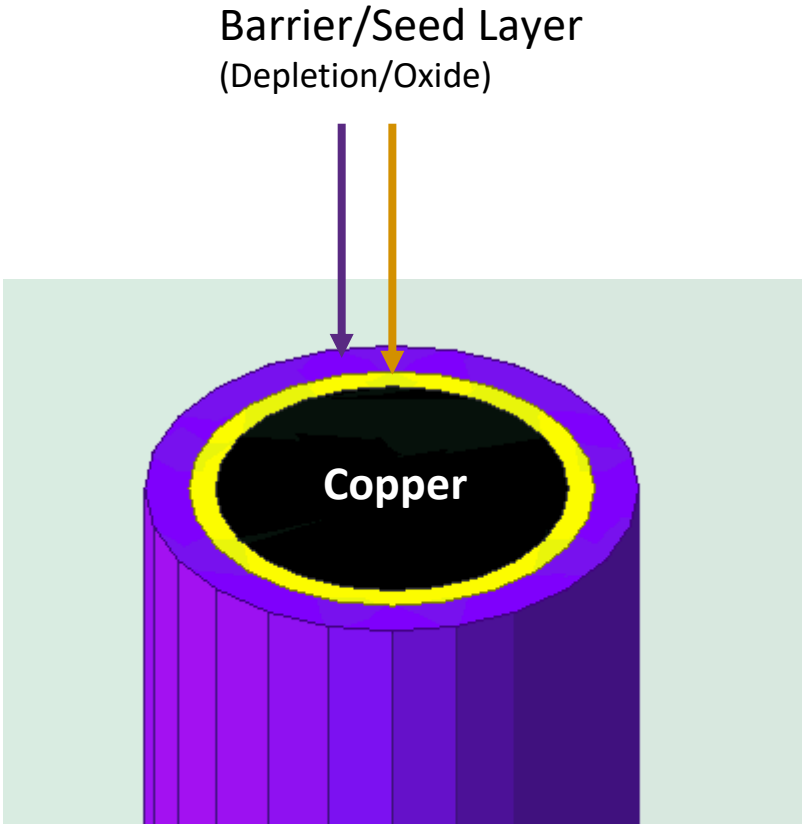
TSV(Through Silicon Via)





HBM SI sign-off with RLC parasitic

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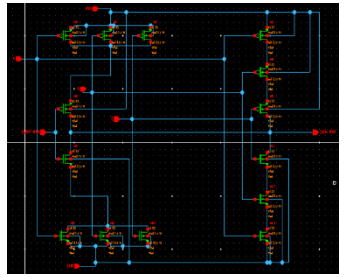
SYNOPSYS® HSPICE®

Synopsys StarRC

Ansys Q3D Extractor
Multiphysics Parasitic Extraction & Analysis



Schematic/Netlist Circuit

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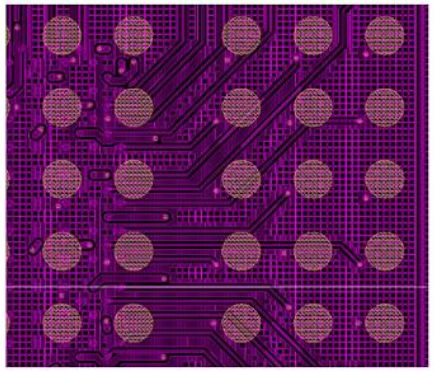

2.5D Die Layout RLC parasitic

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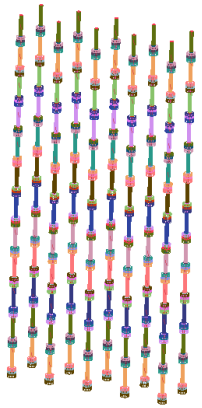
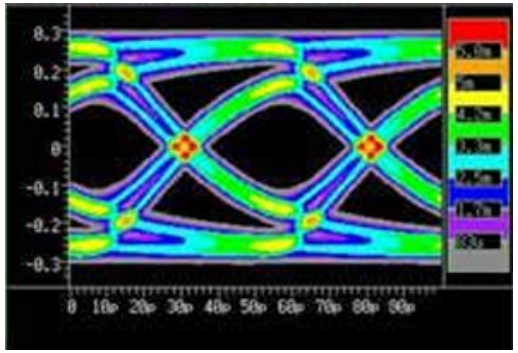


3D TSV RLC parasitic



DDR EYE sign-off

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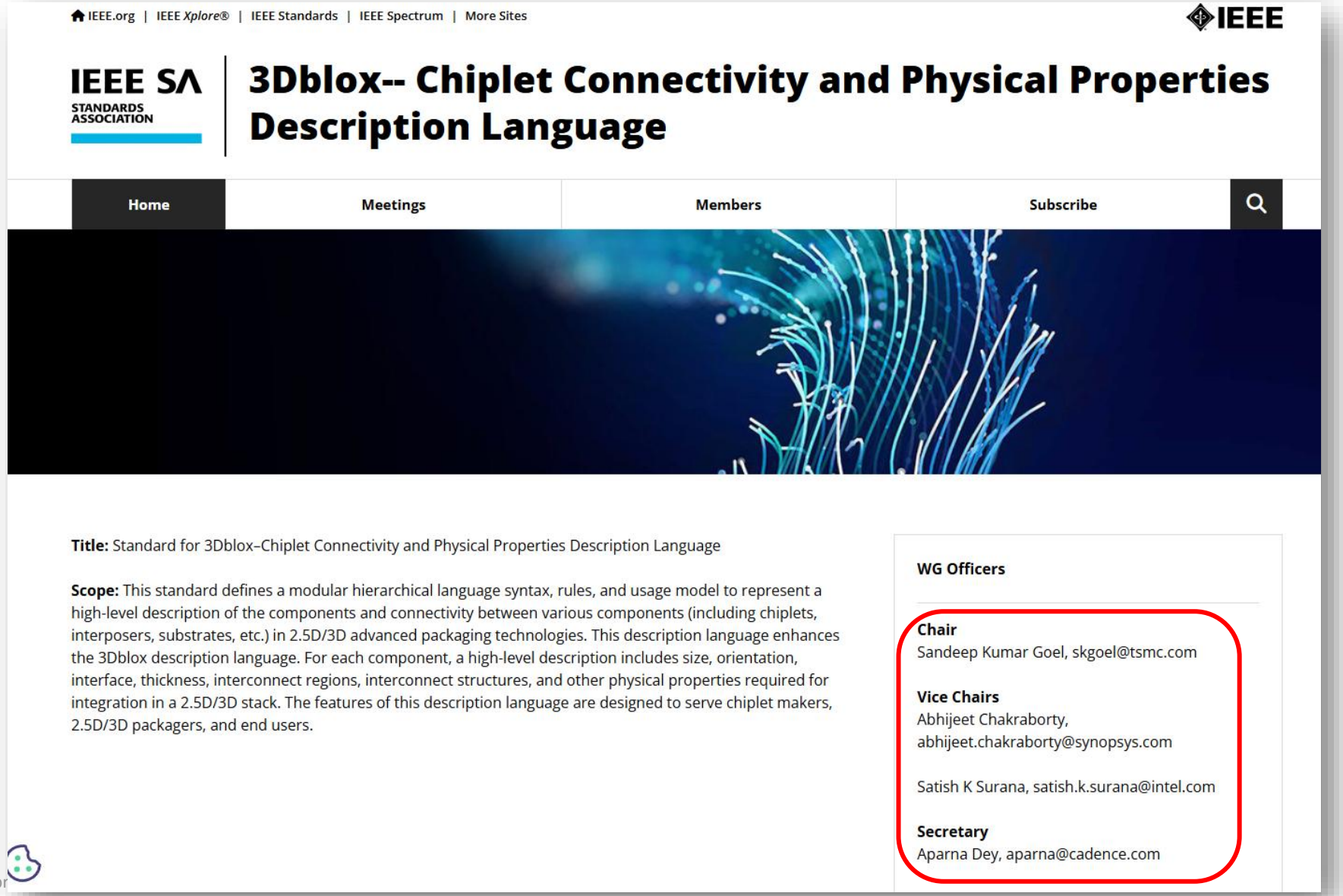
3Dblox 2.0 for Synopsys 3DIC compiler

- **3DFabric** : CoWoS, InFO, SoIC brand name of TSMC
- **3Dblox 2.0** : HBM Design Rule Set for Sigh off (a.k.a Integra)
- 3Dblox 2.0 consists of 5 Parts.

1. Power & Thermal Reliability
2. Physical & Logical Connectivity
3. SI/PI
    - IR drop, Thermal-aware PI
    - Extraction : RLC extraction from TSV, Micro-bump, RDL
    - Insertion loss & Return loss
4. Static Timing Analysis
5. Structural Integrity & ESD

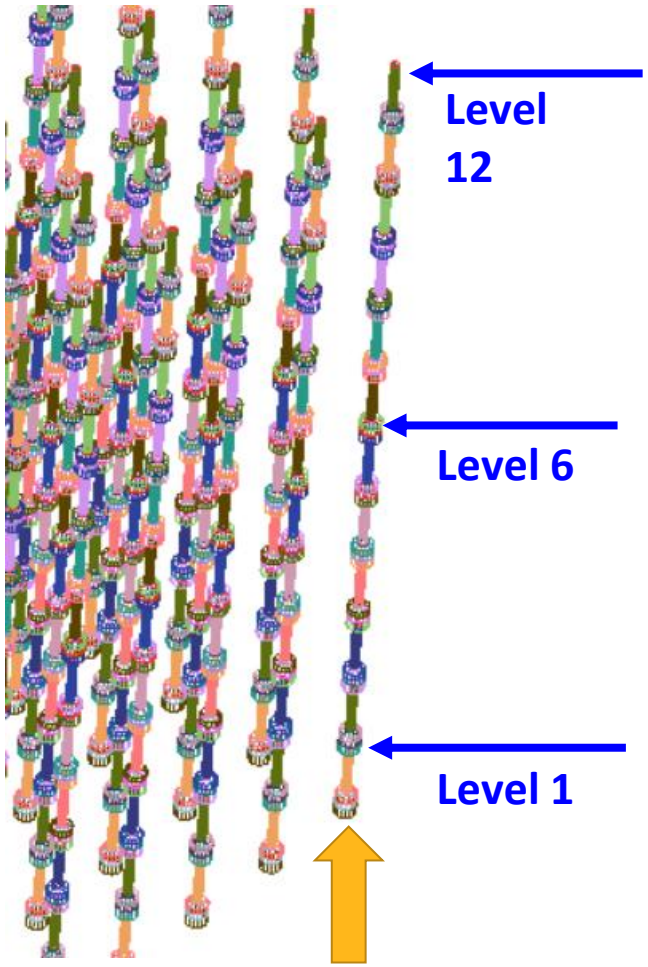
3Dblox official site in IEEE (https://sagroups.ieee.org/)

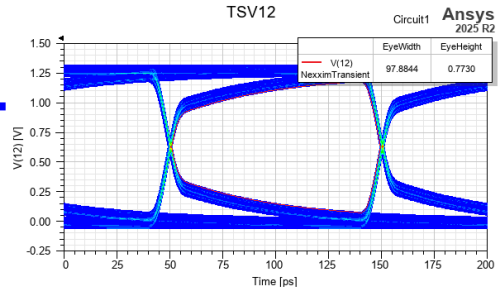


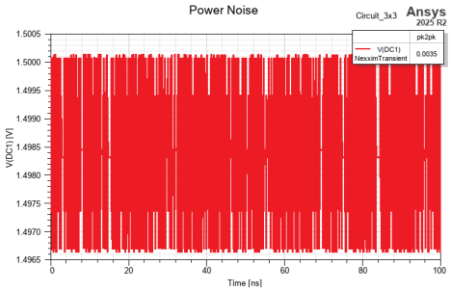
Challenges : TSV design for HBM

- **Too many TSVs**
  - HBM4 has over 8000 TSV with 12stacks
  - Budden of modeling, slow GUI rendering
  - Too long analysis time
  - slow and time-consuming post-process.
- **Optimum TSV assignment**
  - What is optimum assignment of Signal, Power, GND ?
  - How to optimize TSV assignment ?
- **What is the Key performance ?**
  - EYE & timing margin
  - SSN
  - TSV inductance

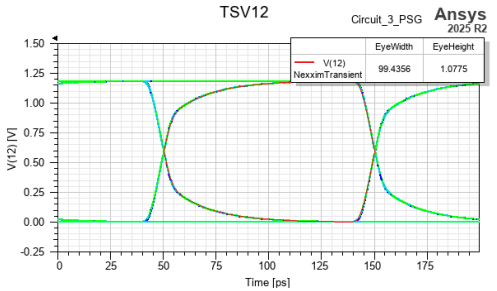
HBM4 TSV : Power noise (SSN) Issue

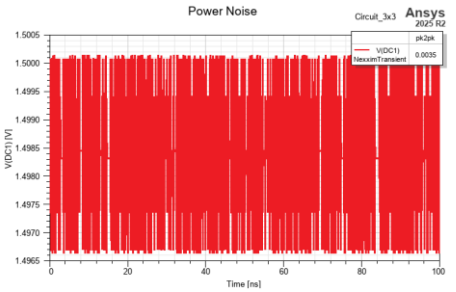




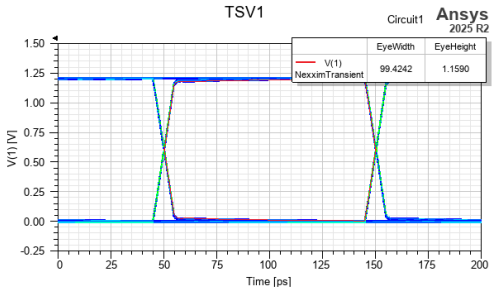


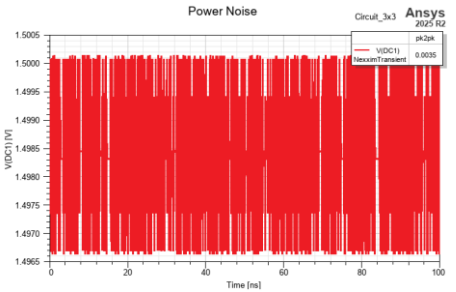
14 mVpp





7 mVpp

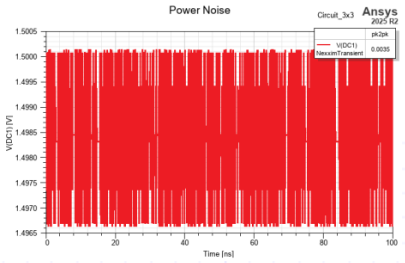


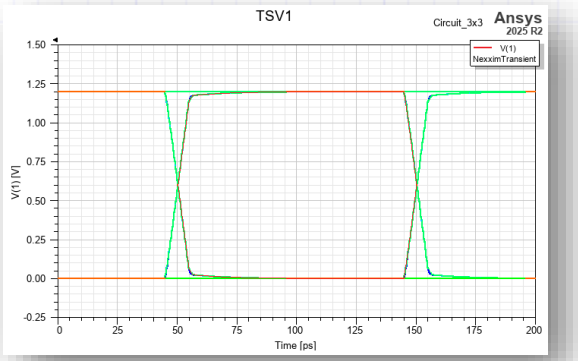


3 mVpp

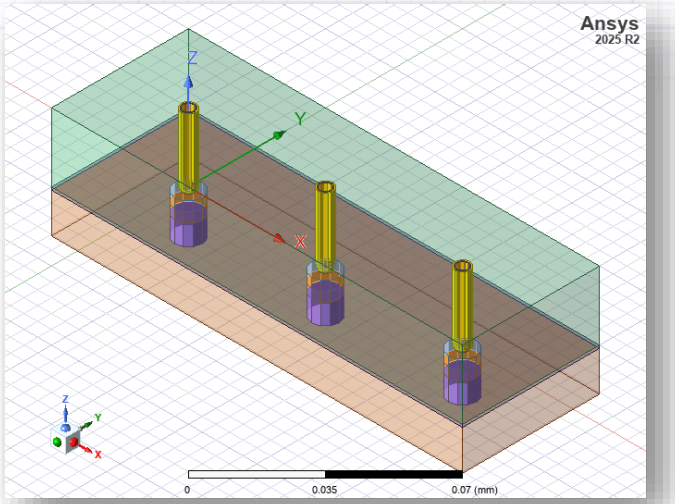
- High level node of TSV shows worse performance (DQ timing margin, SSN) due to increased **total inductance** through TSV path.

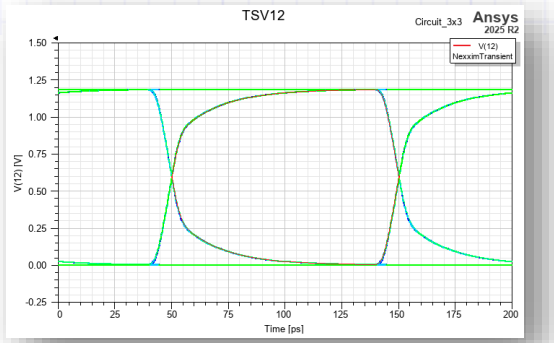
SSN test with 12stack TSV





Level 1





Level 12

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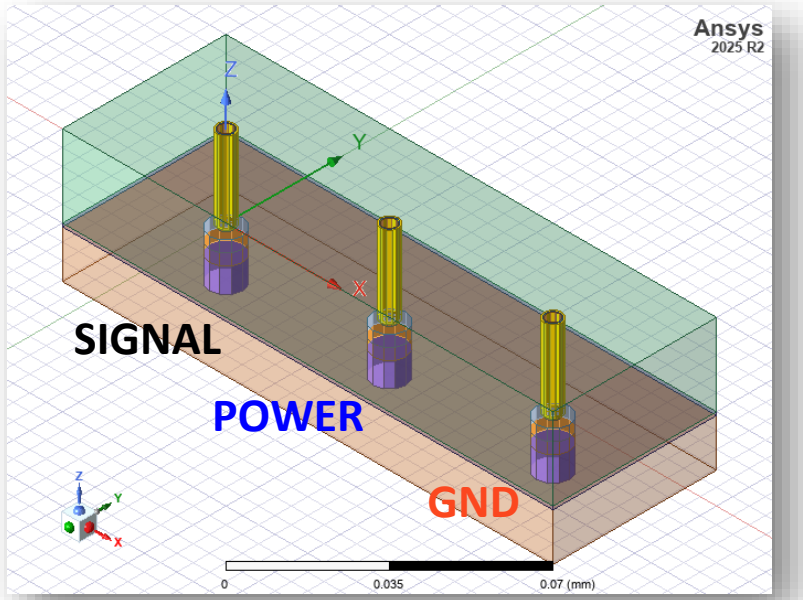
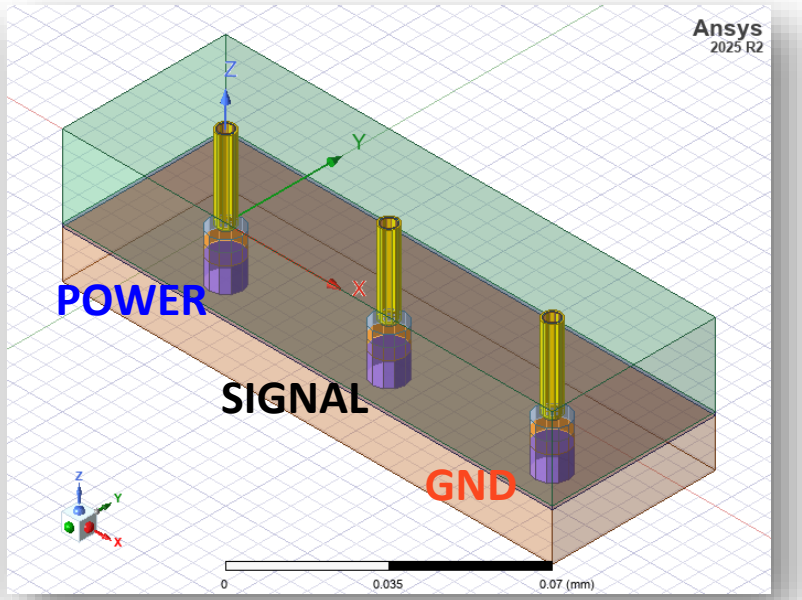
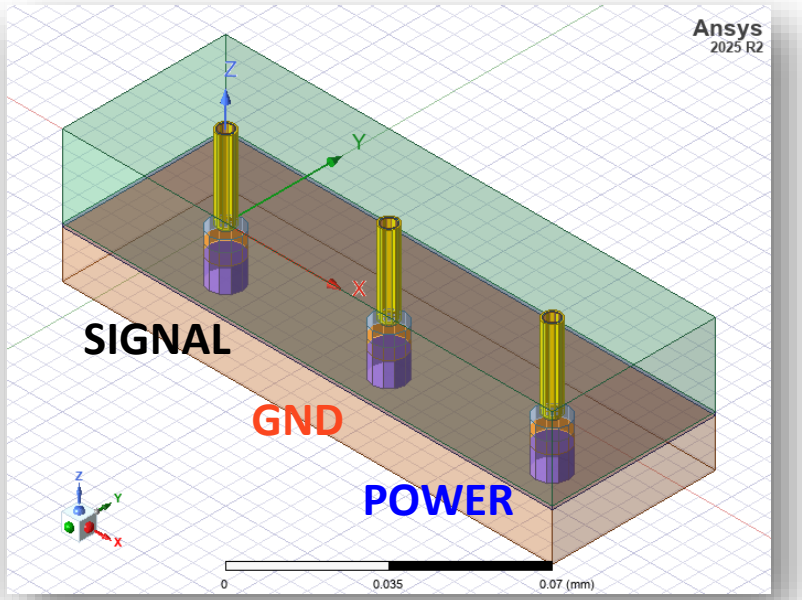
SSN test with 12stack TSV : Result



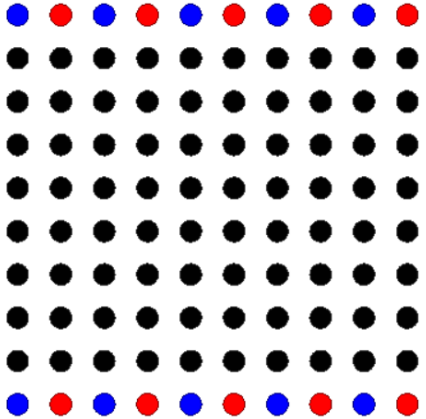




Unit : mVpp	S-P-G	P-S-G	S-G-P
Level 1 Power ripple	3.5	3.5	**1.9**
Level 12 Power ripple	14.5	14.7	**4.5**

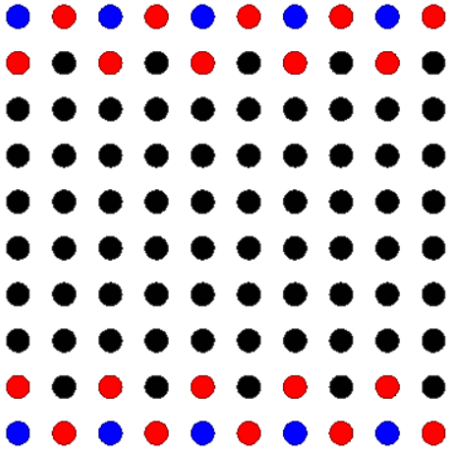
Optimum Pin Array (Example)

Minimum PDN

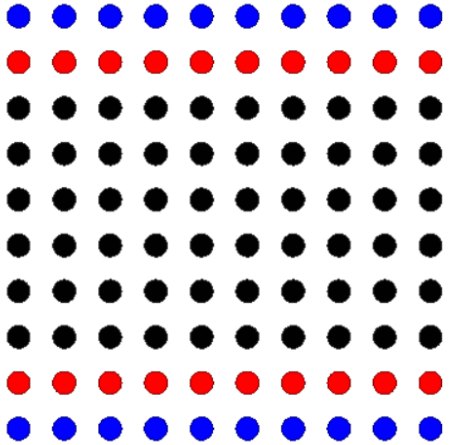


- P/G : 10% of total

S-G-P Ground guard



- P/G : 15% of total



- P/G : 20% of total

Signal Power Ground

- All Pin(TSV or Microbump) would be extracted as signal in Q3D
- Signal/Power/GND could be assigned to each TSV at circuit analysis to optimize it

Ansys part of SYNOPSYS®

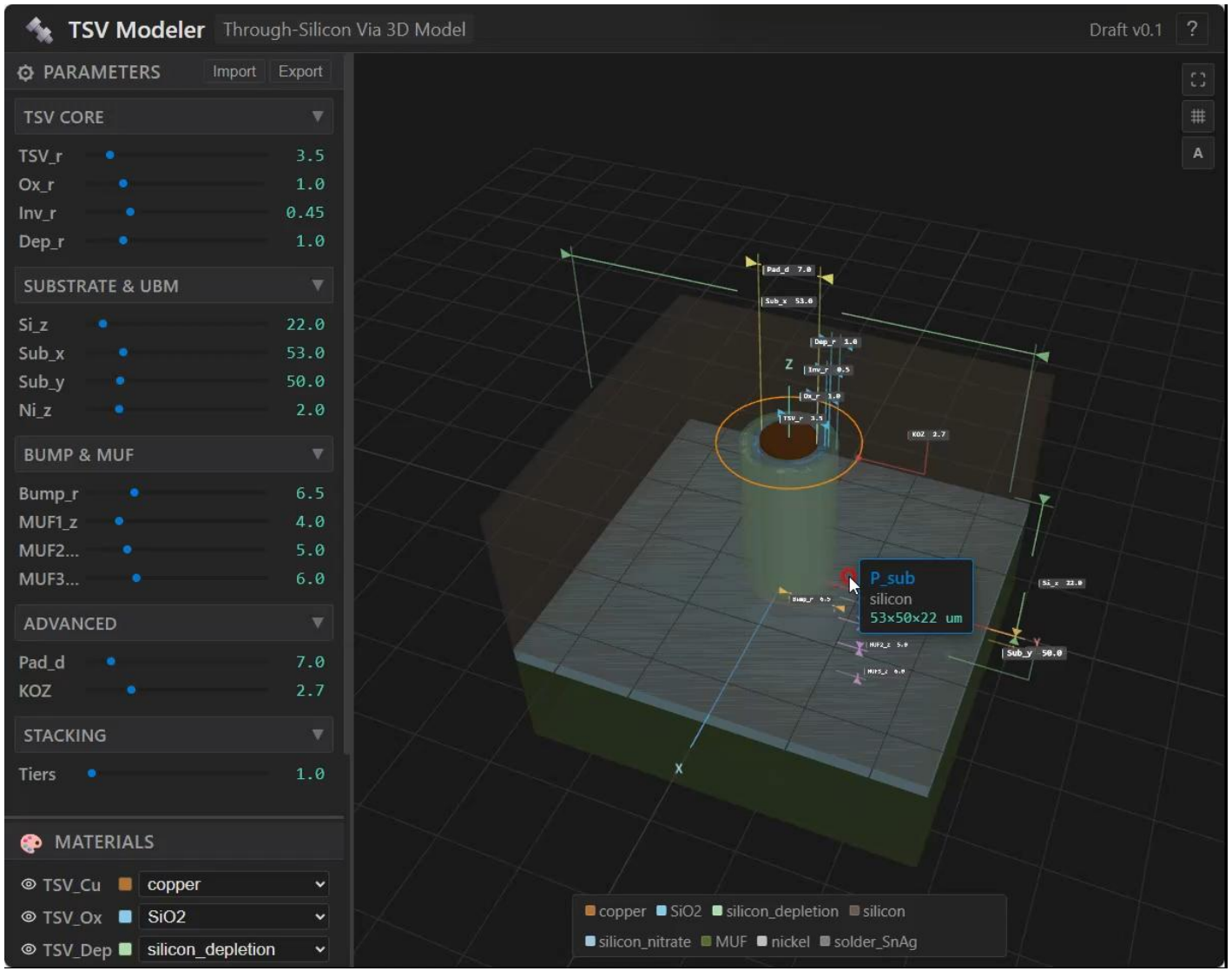
Needs for automation

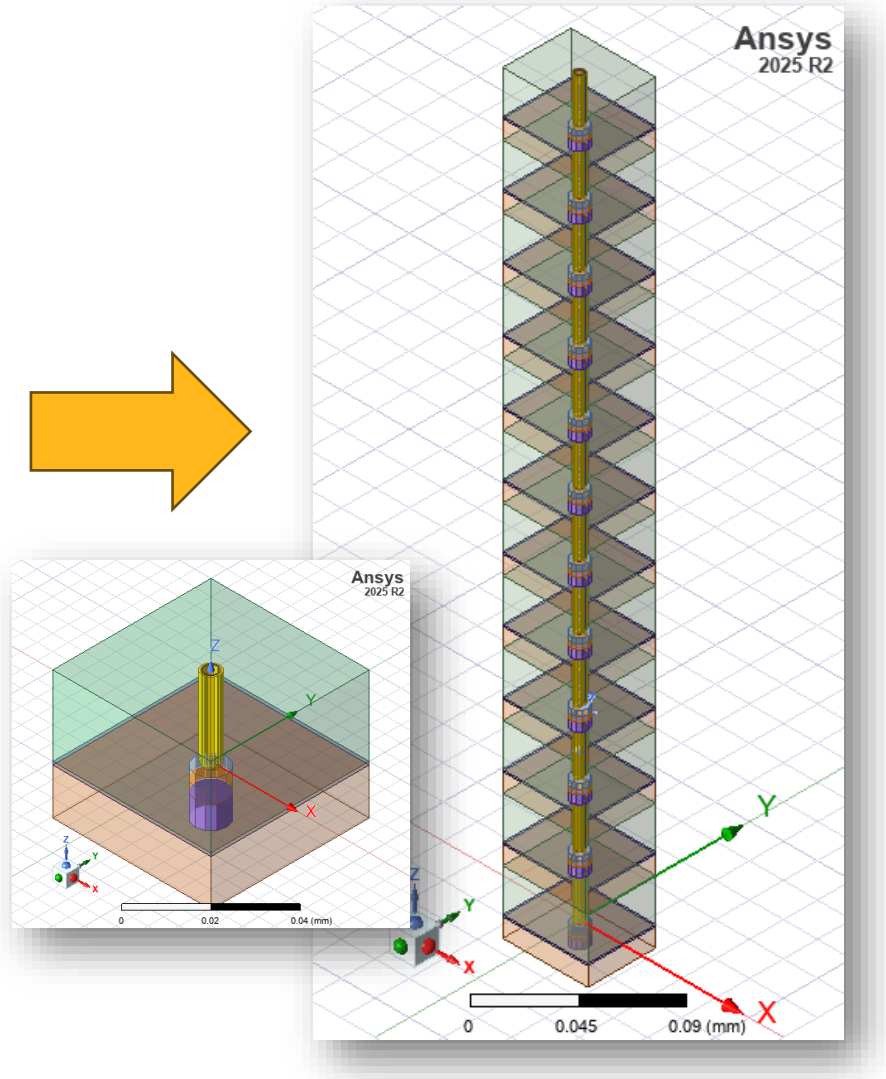
- **Non-GUI process**
  - Slow rendering due to complex 3D model like as 1000 TSVs
  - From pre-processing to analyze & post-processing

- **Array based on X,Y coordination data**
  - Microbump/TSVs should be located at arbitrary/proper position

- **RLC/SPICE reduction & export**
  - Huge size of SPICE/RLC from the bunch of terminal
  - Needs for RLC threshold control / reduce order

Automatic TSV modeling with variable





- Generate fully parameterized TSV model

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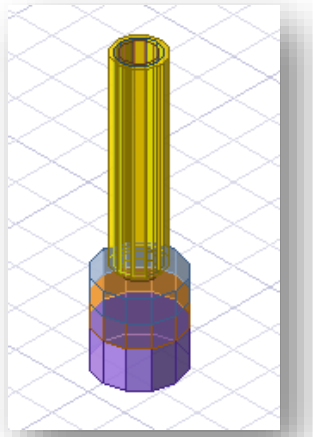
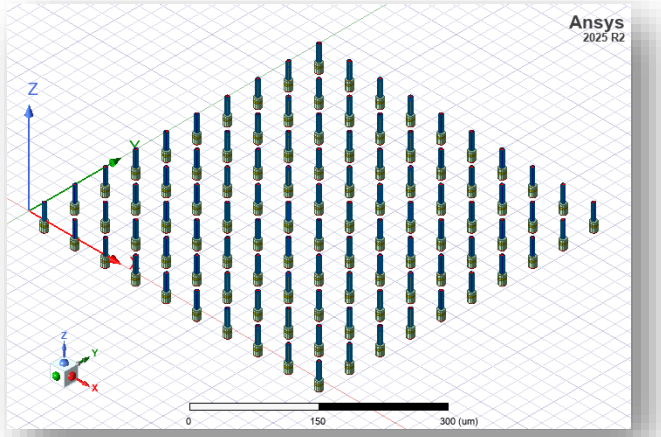
Key Automation : TSV/uBump array based on X,Y coordinate data

Uniform

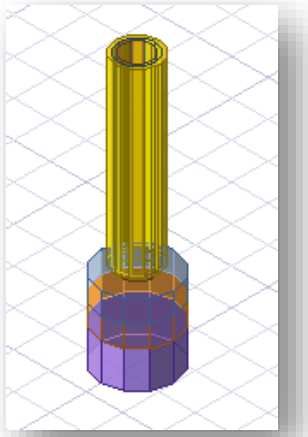


Manual duplicate

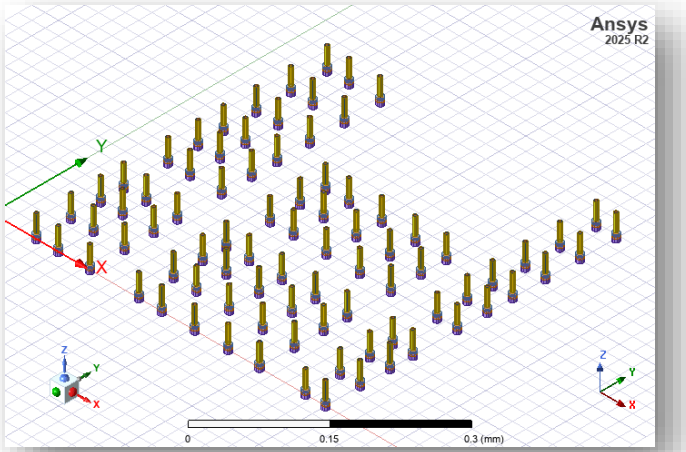


- Rectangular & uniform spacing

Arbitrary



Placement based on X,Y coordinate data



- Arbitrary shape & spacing

it's nearly impossible by manual due to..
- too many TSVs
- slow GUI rendering
- extremely time consuming

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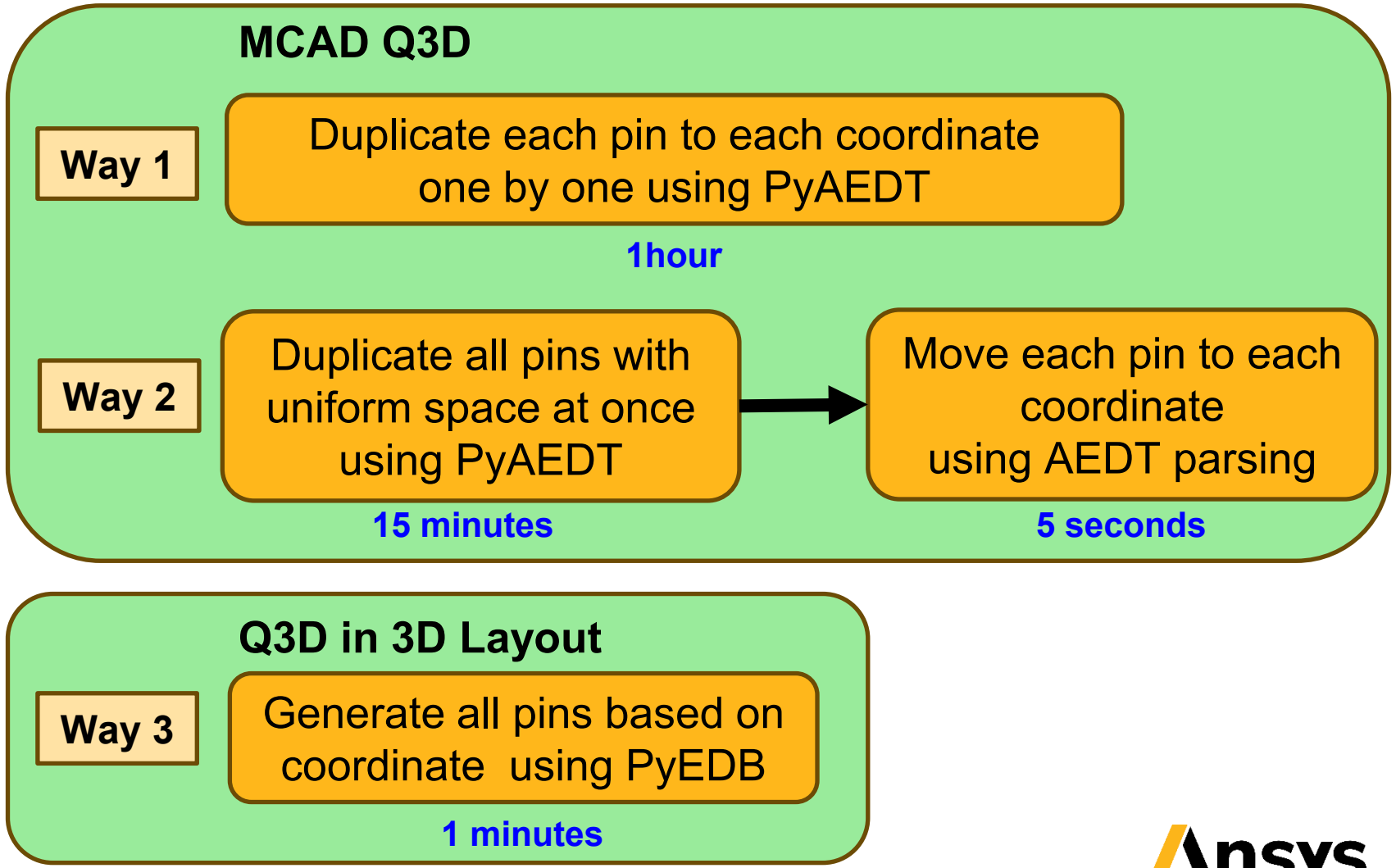
Algorithm for pin array based on X,Y coordinate

* 1000 pins case example

Base model (TSV / ubump)

X,Y coordinate data



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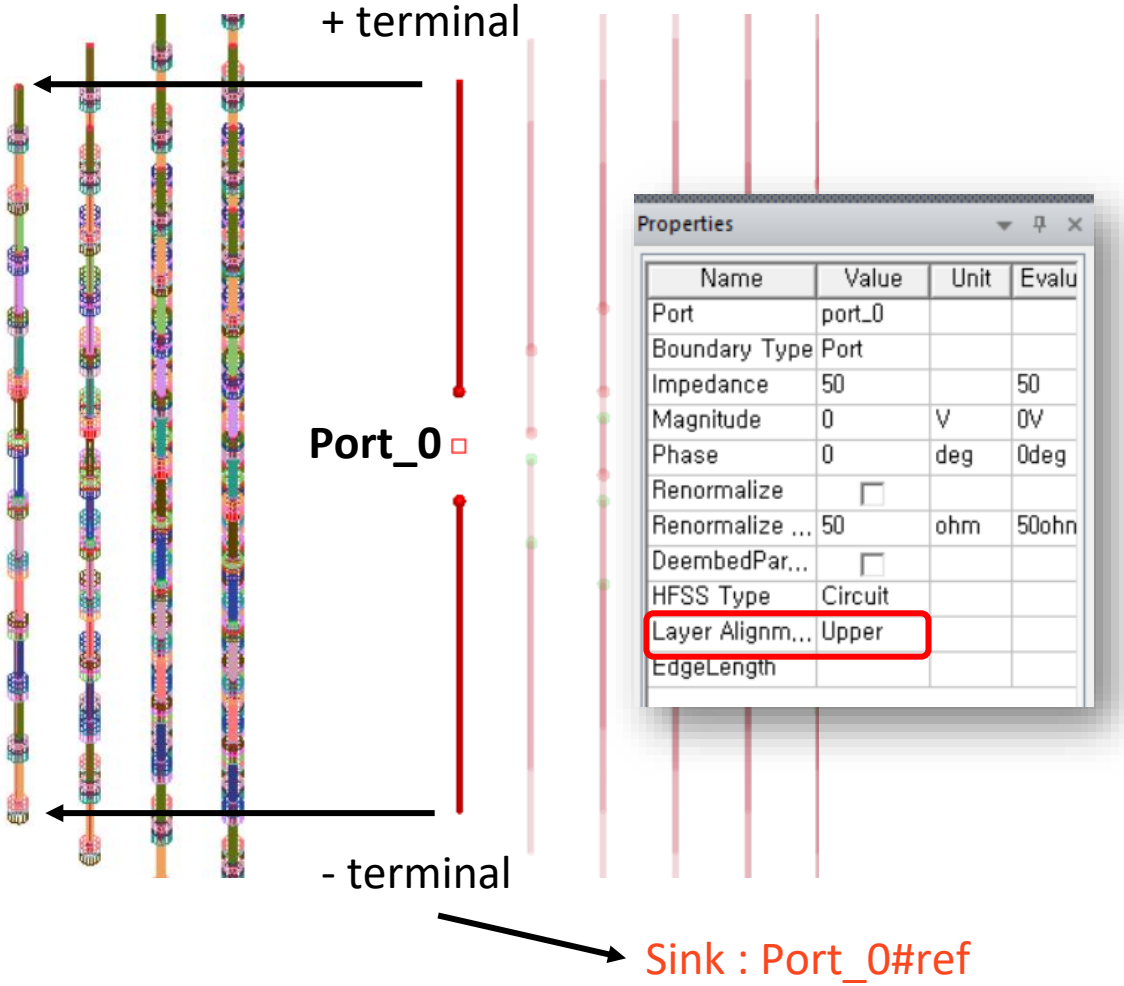
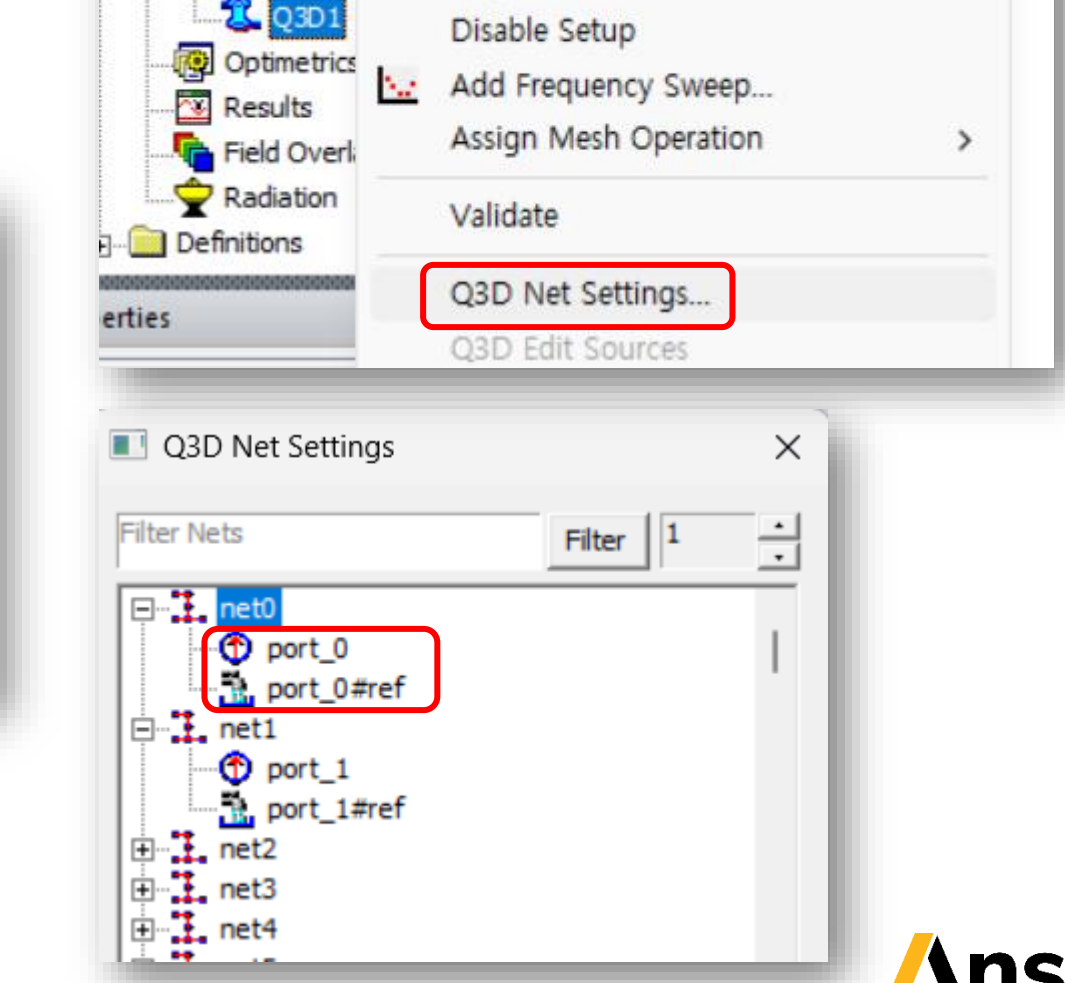
Automation : MCAD Q3D vs. Q3D in 3D Layout

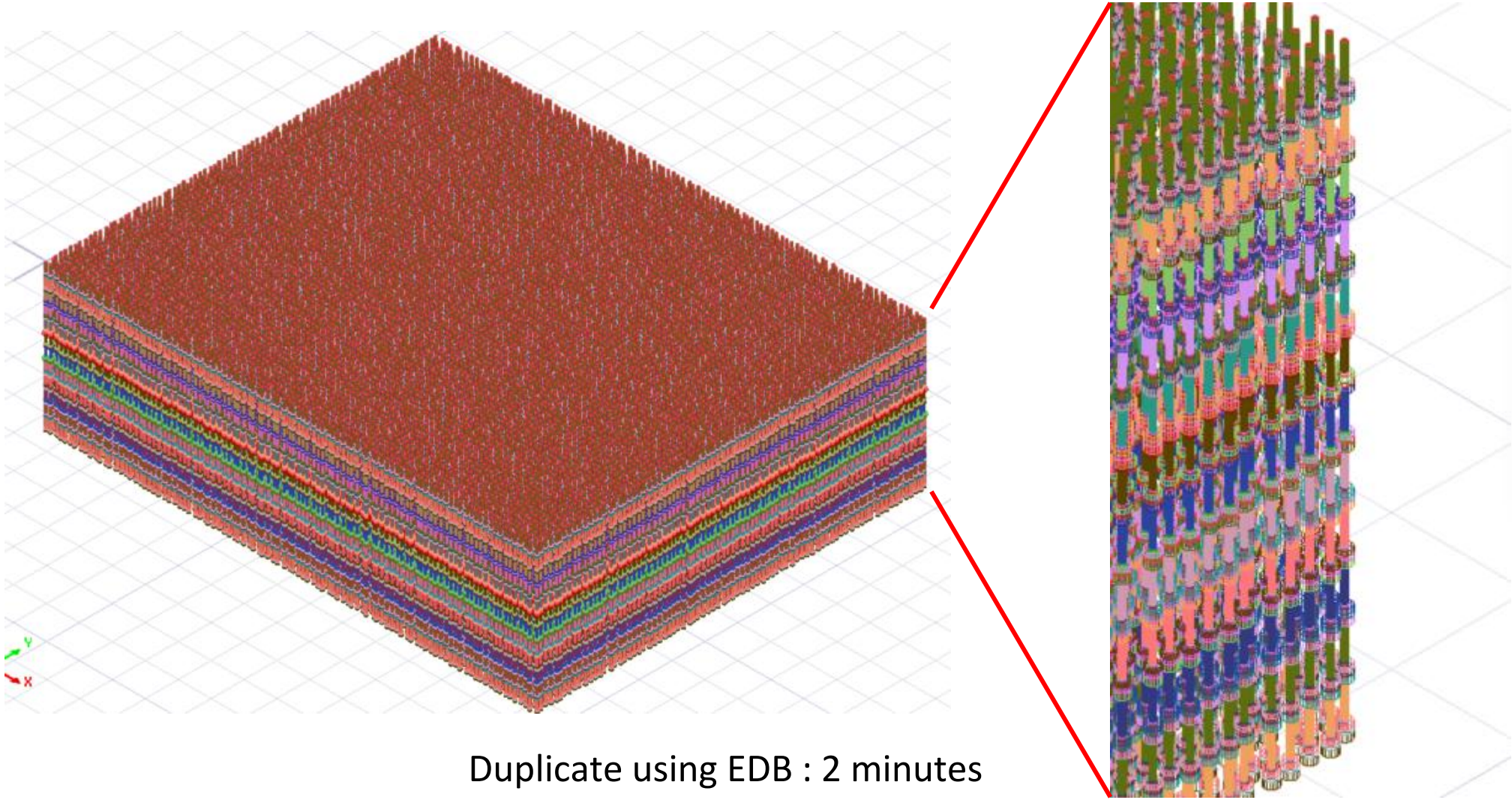
	MCAD Q3D	Q3D in 3D Layout
Main API	PyAEDT	PyEDB
Automation speed	Slow (1~8hr)	Super fast (< 2m)
Net/terminal name change	easy	Complex
SPICE/RLC reduction	Use Internal function	Need for hard coding
Assign Source/sink	Easy & Simple	Depends on port property
Reduce matrix	Full function	Limited function

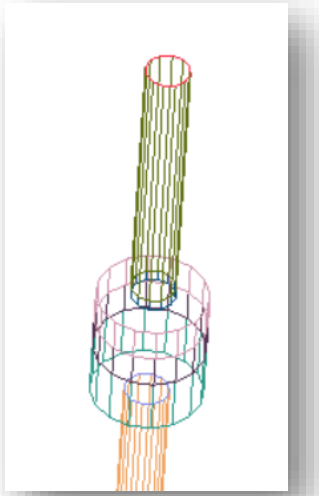
Tip for Q3D in 3D Layout : single circuit port Source & Sink





3DL Q3D Automation Test (8000 ea with X,Y coordinate)



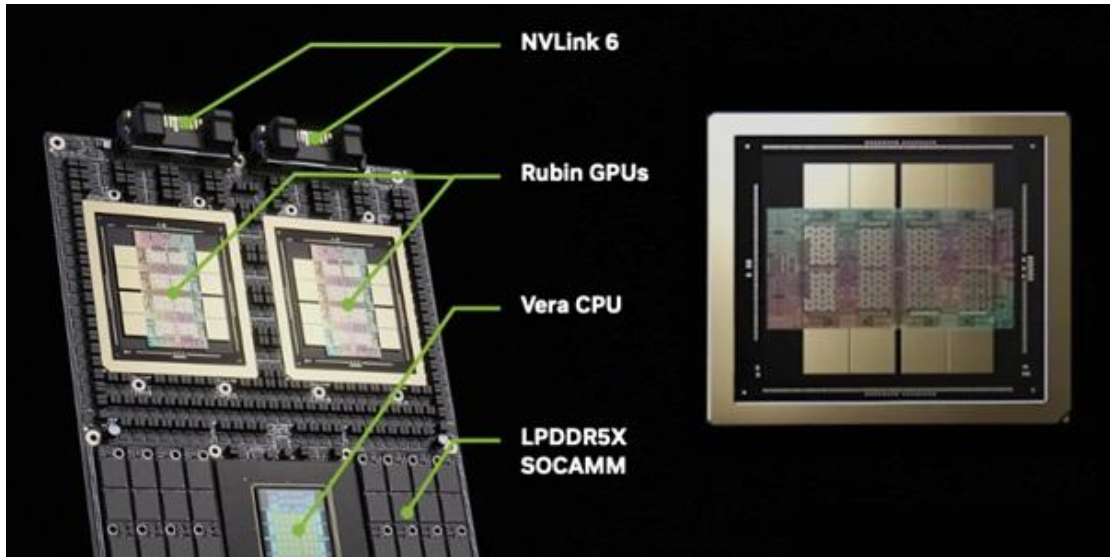


Duplicate using EDB : 2 minutes
open aedb : 3 minutes
AEDT fiel with aedb folder : 100MB

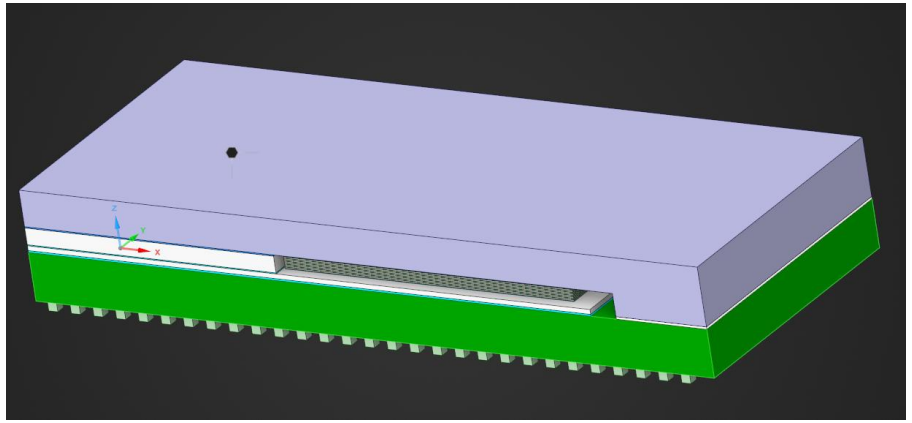
Ansys part of SYNOPSYS®

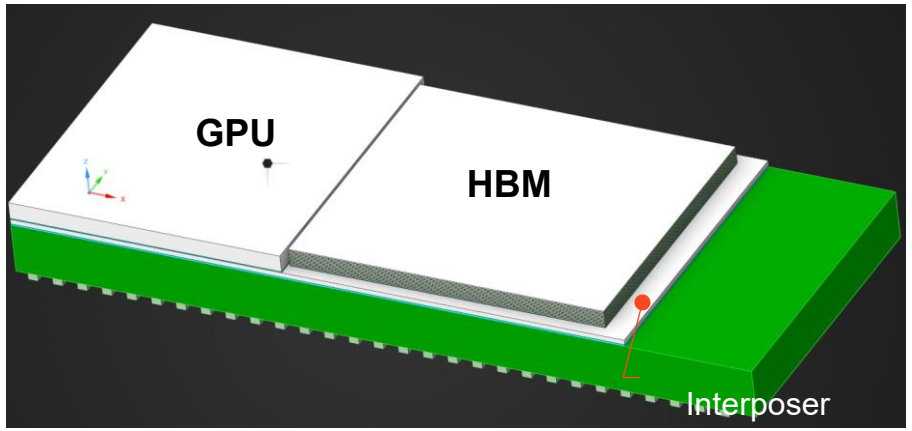
Microbump Thermal Simulation

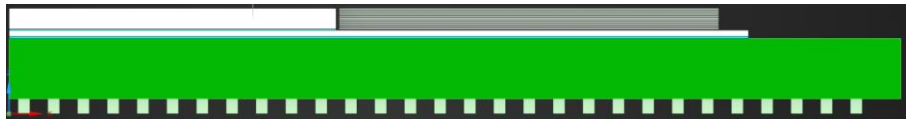
Partial modeling of 2.5D package



Simulation Model →







Ansys part of SYNOPSYS®

HBM4 bump information

JESD270-4A

JEDEC Standard No. 270-4A
Page 202

11.2 MicroBump Positions

The MicroBump array of the DRAM stack employs a staggered pattern as depicted in Figure 104 where a 'staggered' bump is located halfway between major row and column, hence its location is determined by X/2 and Y/2. Table 110 shows geometric parameters of the Staggered MicroBump pattern. Parameter P_{min} is the minimum bump pitch anywhere in the MicroBump field; for chosen X and Y parameters.

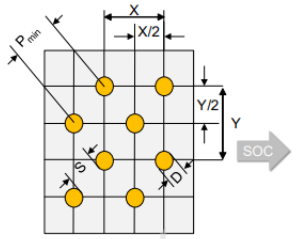


Figure 104 — Staggered MicroBump Pattern

Table 110 — Geometric Parameters of the Staggered MicroBump Pattern

Label	Nominal Value	Description
X	70 µm	Horizontal pitch of two adjacent MicroBumps
Y	110 µm	Vertical pitch of two adjacent MicroBumps
P_{min}	65 µm	Minimum pitch of the bump field
D	28 µm	MicroBump diameter
S		Bump-to-bump air gap; $S = P_{Min} - D$

The HBM4 bump map is defined as shown in subsequent tables. Please refer to MO-362 for device dimensions.

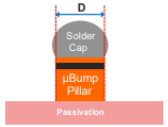


Figure 105 — MicroBump Pillar Diameter

Bump pitch: 65um
Bump diameter: 28um

Table 111 — HBM4 Device Dimensions

Parameter	Symbol	Configuration	Minimum	Nominal	Maximum	Unit	Notes
Width	X	24Gb/die	12.75	12.775	12.8	mm	3,4,5
		32Gb/die	14.15	14.175	14.2		
Length	Y		10.95	10.975	11	mm	
Height	Z	4-High	750	775	800	µm	1, 2
		8-High	750	775	800	µm	
		12-High	750	775	800	µm	
		16-High	750	775	800	µm	

NOTE 1 The configuration refers to the number of memory dies in the stack. The stack may include an additional base (interface) die.
NOTE 2 Refer to MO-362 for related package drawings.
NOTE 3 Refer to MO-362 for X and Y dimension min/Max tolerances and related package drawings.
NOTE 4 Refer to Footprint A in JESD271-4 "High Bandwidth Memory (HBM4) DRAM Bump Map Spreadsheet" for details on the 24 Gb/die footprint.
NOTE 5 Refer to Footprint B in JESD271-4 "High Bandwidth Memory (HBM4) DRAM Bump Map Spreadsheet" for details on the 32 Gb/die footprint.

HBM4 Package dimensions and bump layout

JESD271-4_HBM4_Ballout

Table 111 — HBM4 Device Dimensions

Parameter	Symbol	Configuration	Minimum	Nominal	Maximum	Unit	Notes
Width	X	24Gb/die	12.75	12.775	12.8	mm	3,4,5
		32Gb/die	14.15	14.175	14.2		
Length	Y		10.95	10.975	11	mm	
Height	Z	4-High	750	775	800	µm	1, 2
		8-High	750	775	800	µm	
		12-High	750	775	800	µm	
		16-High	750	775	800	µm	

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Bump map FootprintA

11.4 HBM4 Bump Map (cont'd)

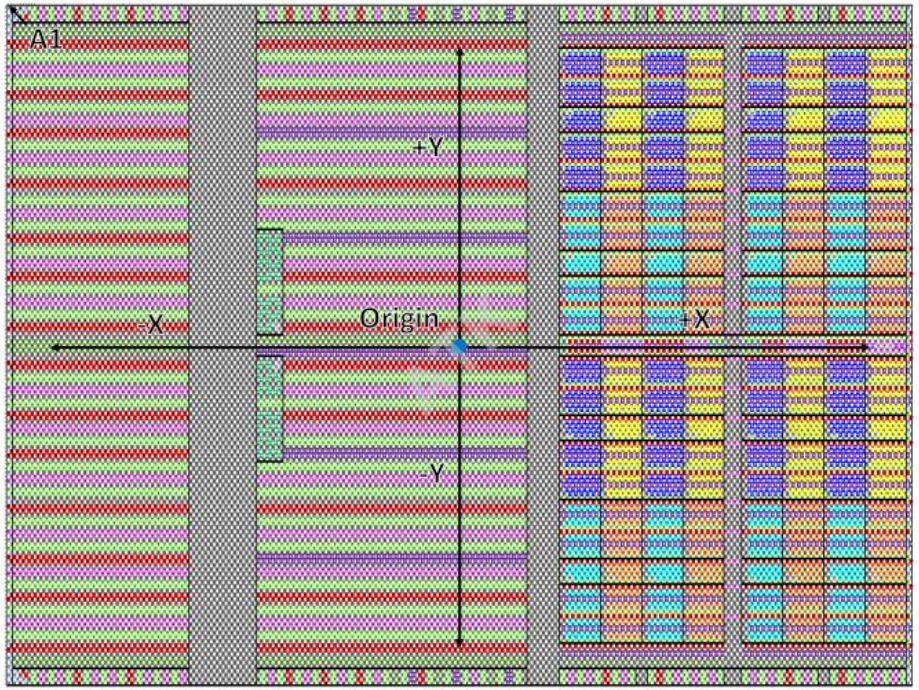


Figure 107 — Overview of HBM4 Bump Map Footprint A

ECAD import

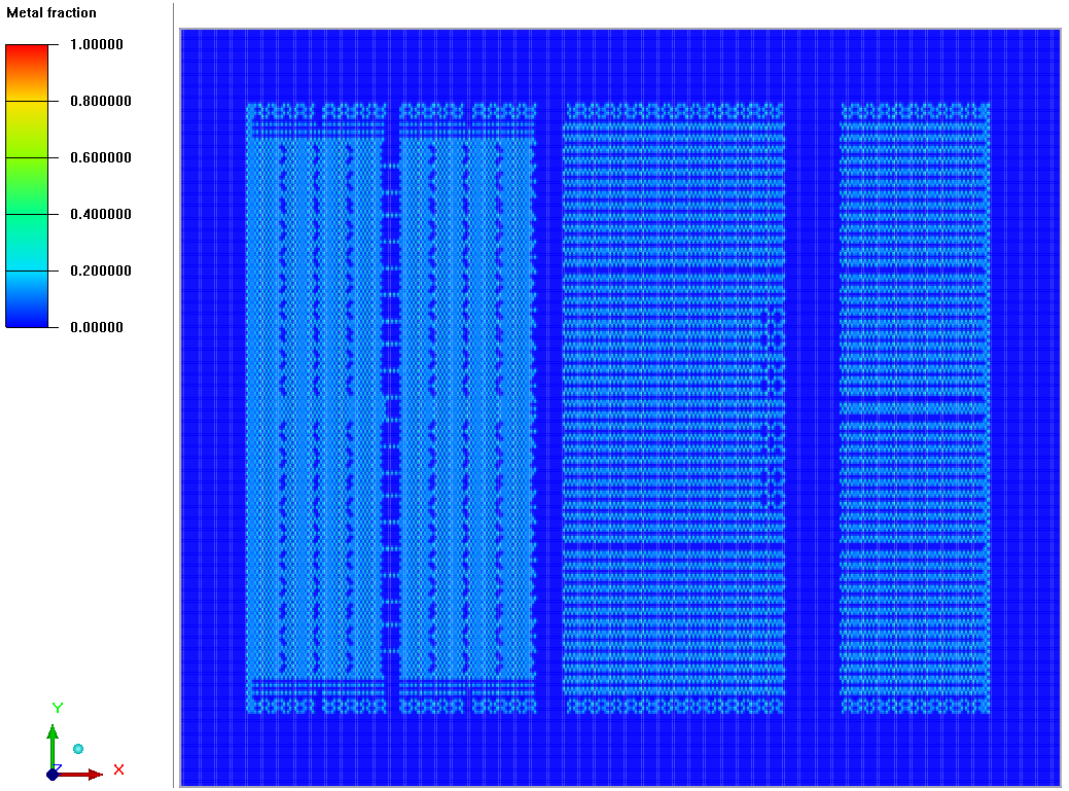
Bump coordinate (x, y)

HFSS 3D Layout or SiWAVE
- ECAD generation

Export ECAD
- (Anf, edb, etc,)

ECAD Import into Classic Icepak

ECAD import

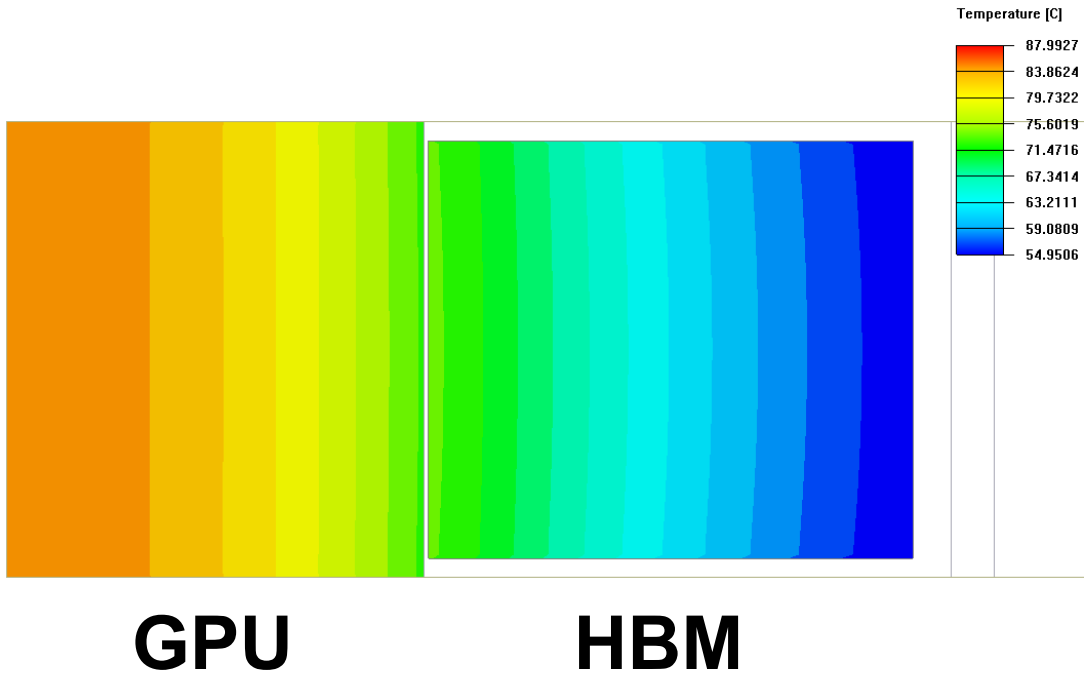


Metal fraction

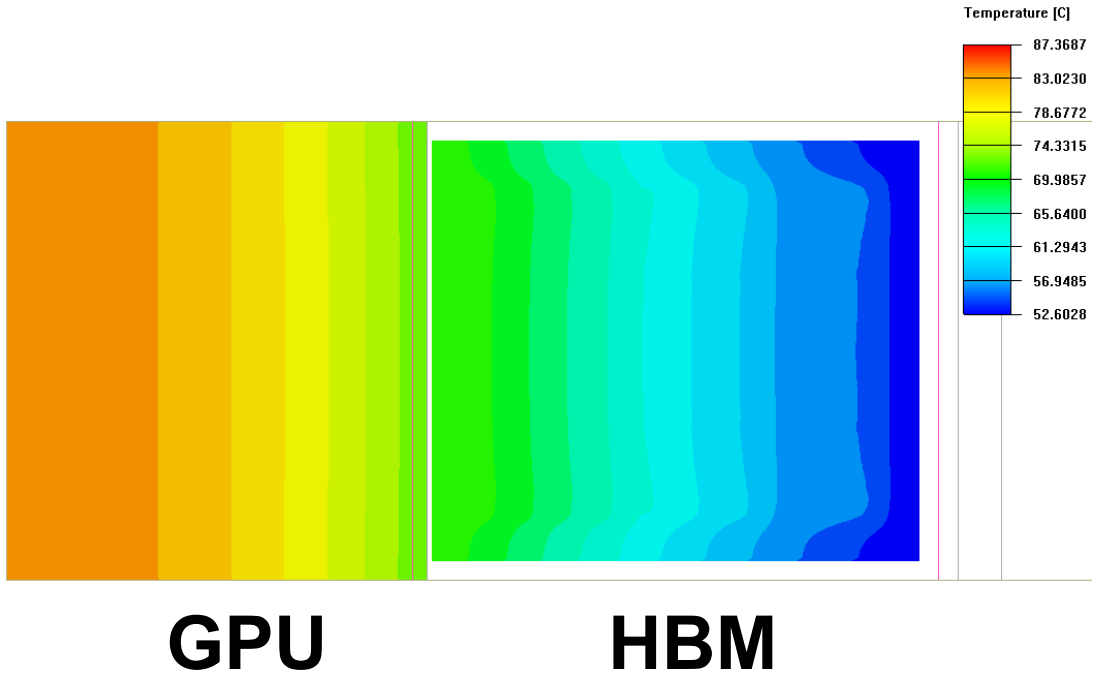
Ansys part of SYNOPSYS®

Temperature contours on GPU and HBM dies

Lumped HBM bump



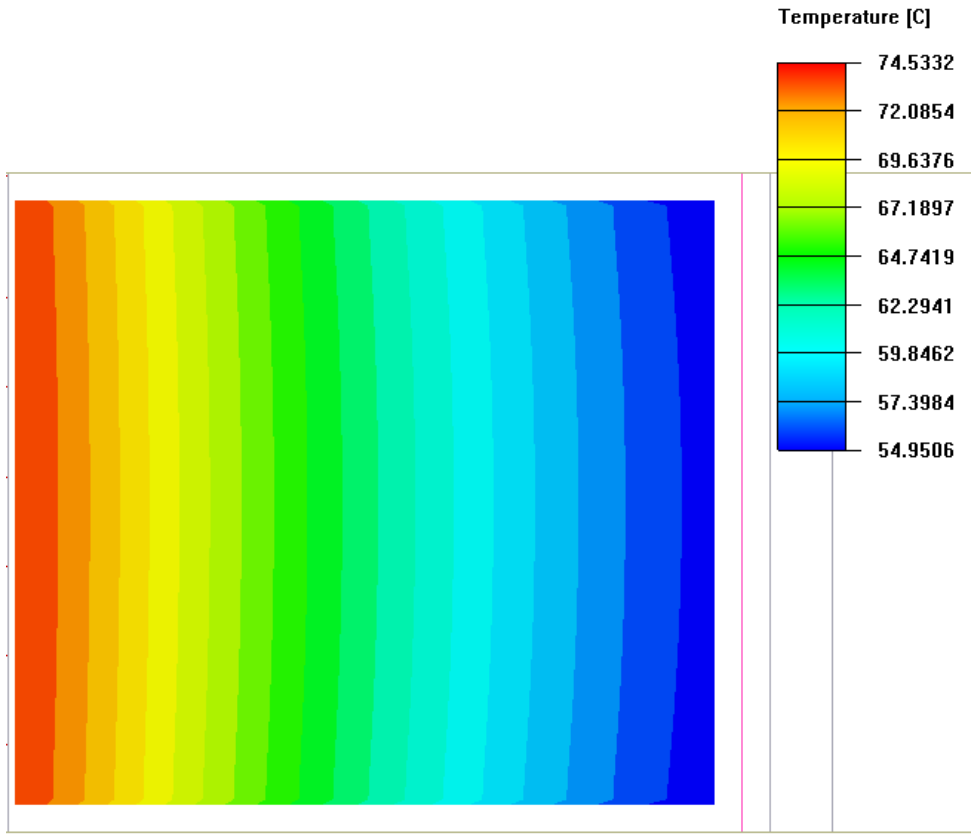
ECAD imported HBM bump (Real bump array based on coordinate)



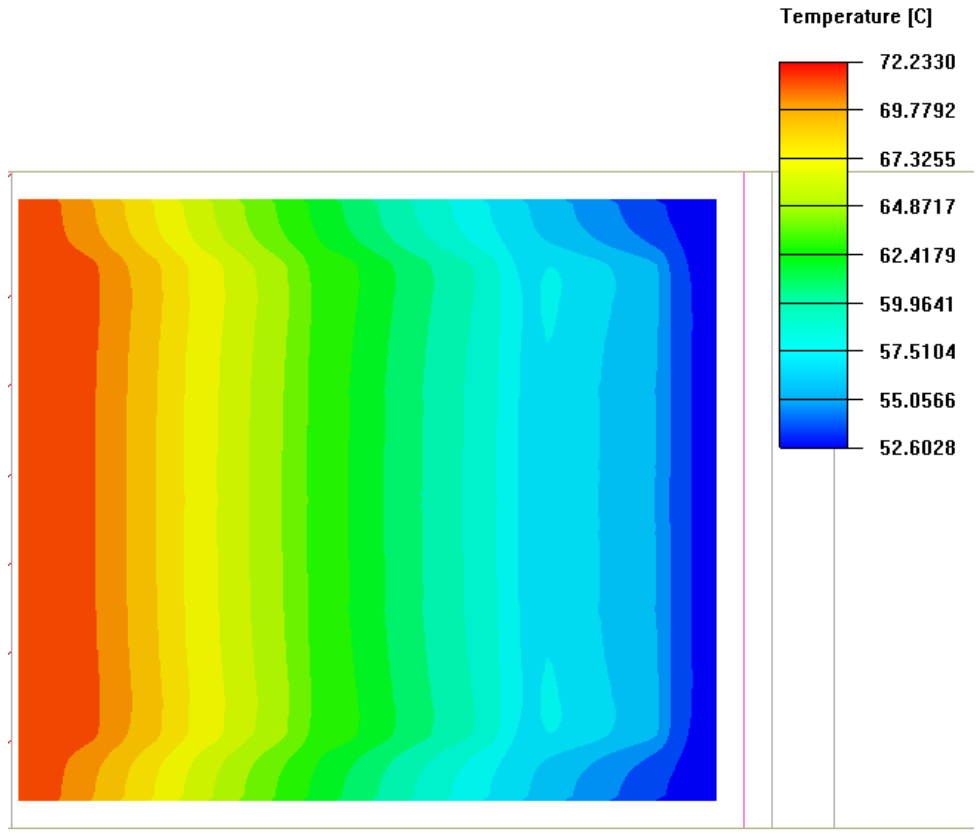
Ansys part of SYNOPSYS®

Temperature contours on HBM dies

Lumped HBM bump



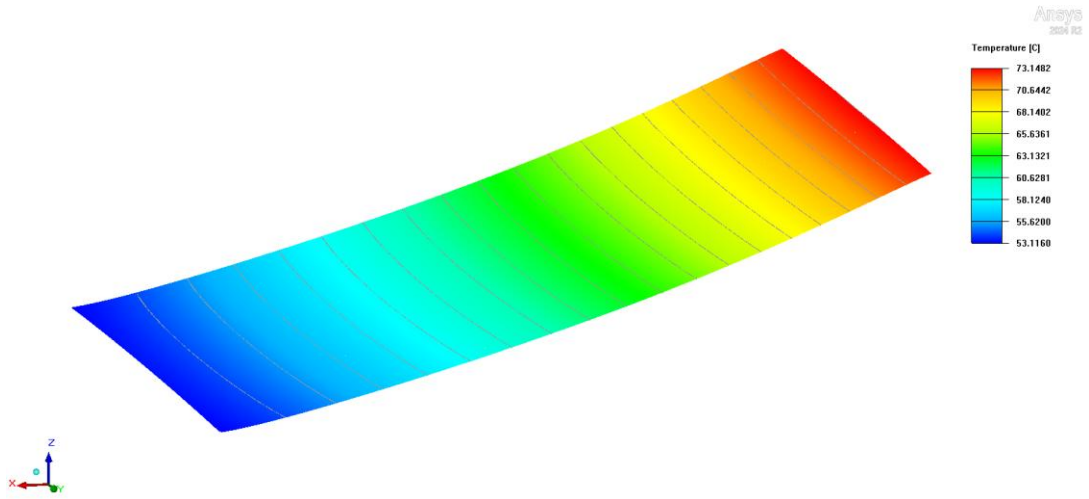
ECAD imported HBM bump (Real bump array based on coordinate)



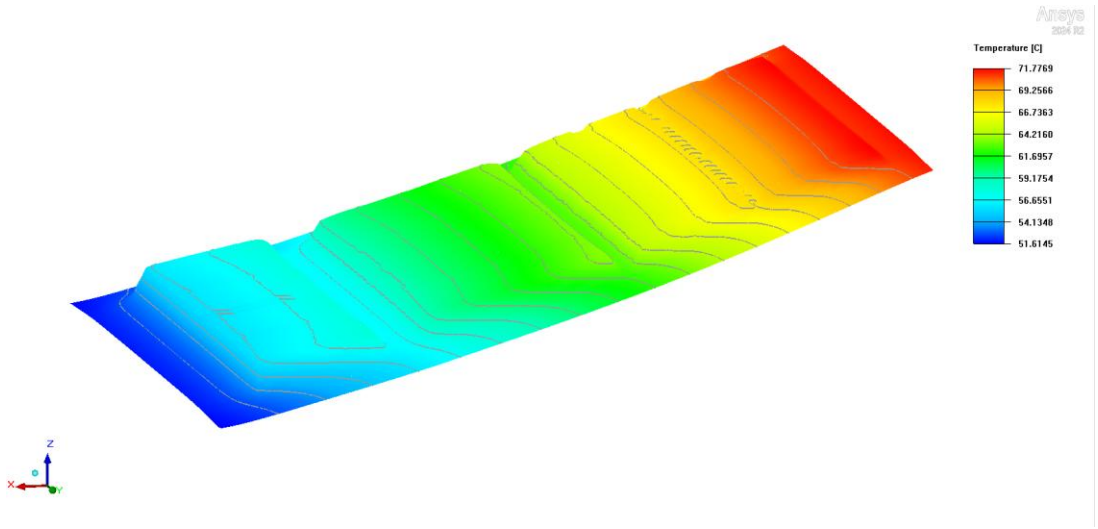
Ansys part of SYNOPSYS®

Temperature contours on HBM dies

Lumped HBM bump



ECAD imported HBM bump (Real bump array based on coordinate)



Conclusion

- **Q3D in 3D Layout can be advanced solution for HBM/3DIC application**
- **TSV parasitic analysis became a very important performance parameter for HBM design**
- **Need for automation for coordinate based TSV/Microbump design.**
- **Proper TSV/Microbump array should be designed based on coordinate for SI & Thermal performance**