Next Gen High Performance Integrity :

Advanced Silicon/Package/PCB Interconnection Design

Chip/PKG/PCB 설계에서의 SI/PI 관련 기술 이슈와 시뮬레이션 Tips & Solutions 및 SI/PI 통합 검증 솔루션 및 방향

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010-3381-1417, sijeung@huwin.co.kr

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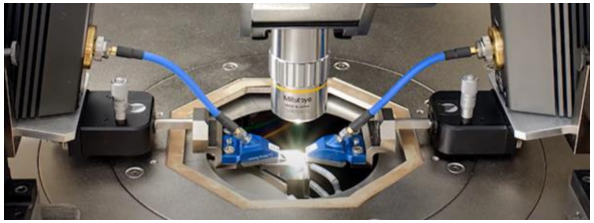
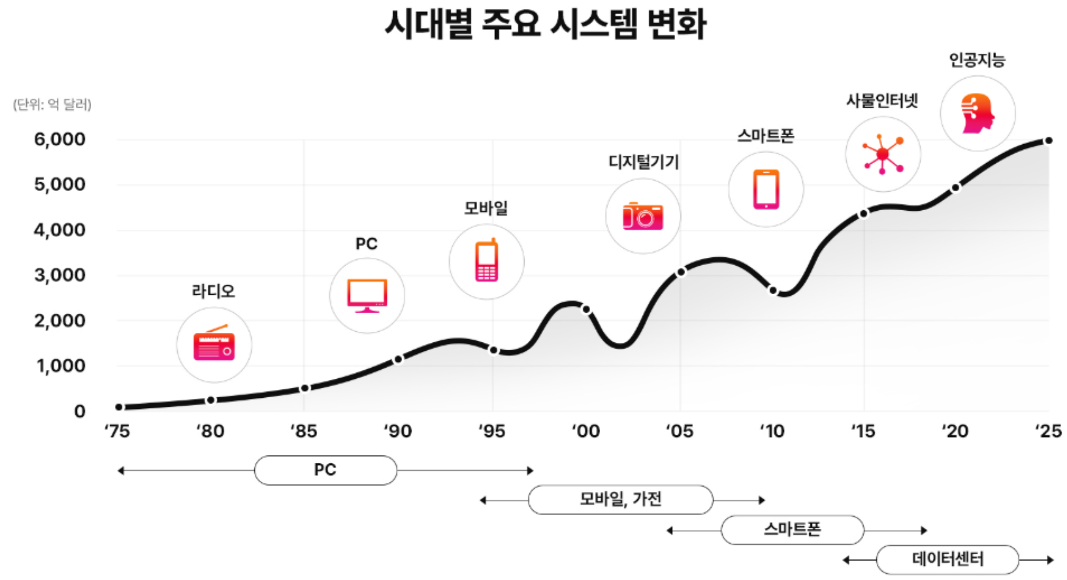
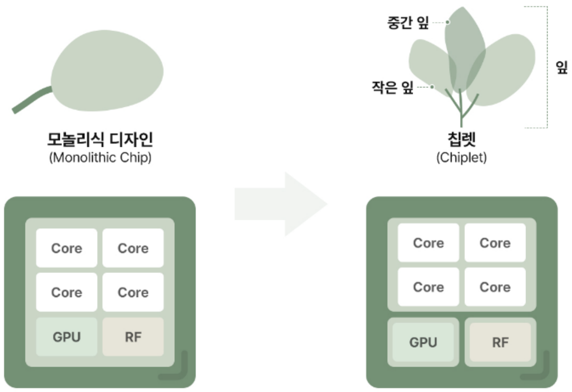
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향
2. 시뮬레이션 통한 SPGTI 설계
3. DesignCon2026 자료 소개

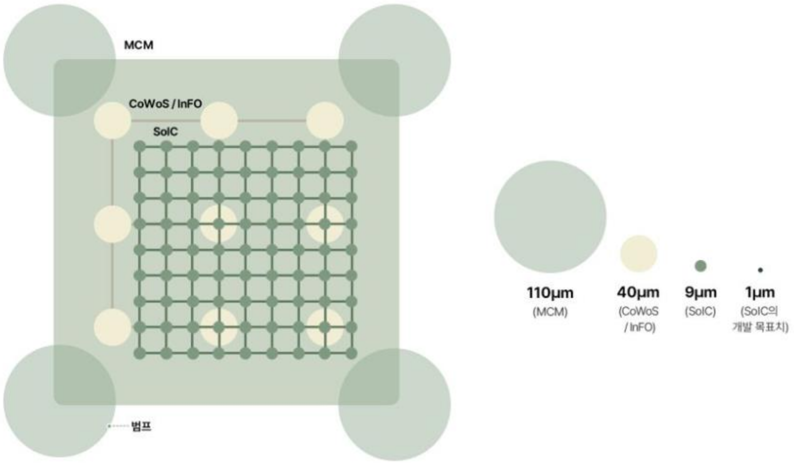


1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 :

반도체 산업의 새로운 챕터, 칩렛 :



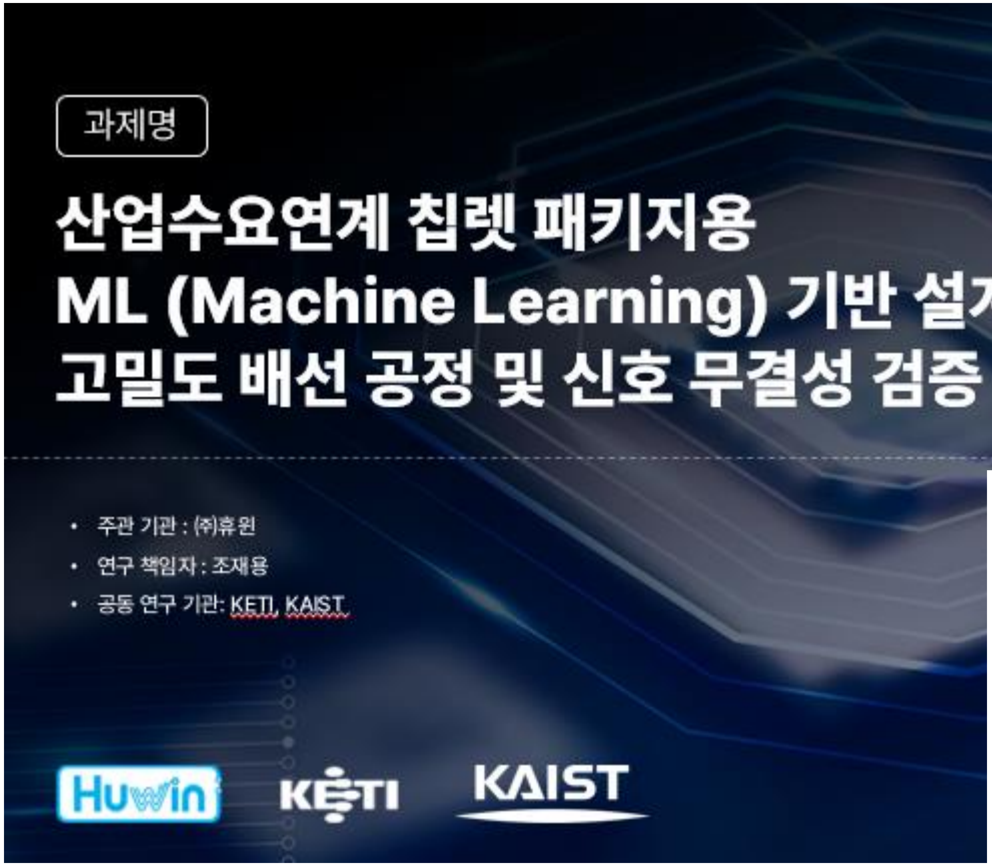




그림출처 : https://news.skhynix.co.kr/packaging-x-files-ep1/

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 :

반도체 산업의 새로운 챕터, 첨단 칩렛 패키징 :



과제명

산업수요연계 칩렛 패키지용
ML (Machine Learning) 기반 설계 최적화,
고밀도 배선 공정 및 신호 무결성 검증 솔루션 개발

- 주관 기관 : ㈜휴윈
- 연구 책임자 : 조재용
- 공동 연구 기관: KETI, KAIST

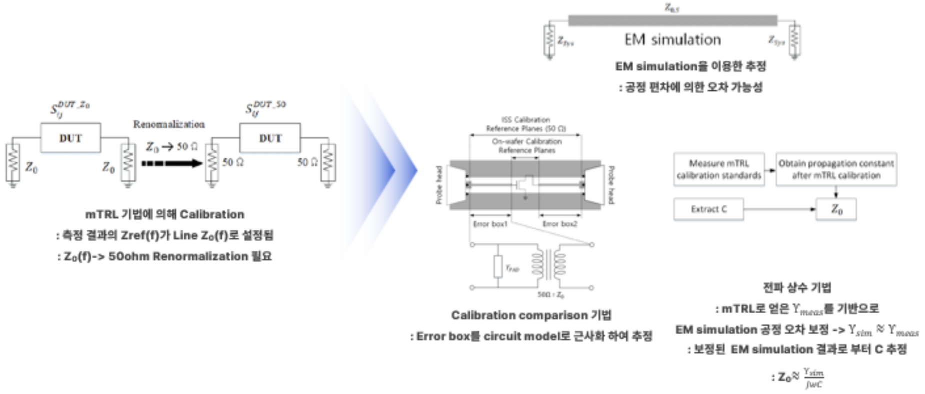
o UCIe 채널의 SI(Signal integrity) 핵심 성능 분석 모듈 개발
o UCIe SI(Signal integrity) 핵심 성능 분석 결과에 대한 Chart 생성 기능 및 Reporting 자동화 시스템 개발

Signal integrity 분야에 특화된
Channel 구성 Ux 및 전처리 기능
(1차년도 항목)

UCIe 채널의 SI 핵심 성능 분석 기능 개발
: VTF, IL/RL, TDR, TDT 등
: PI 분석 모듈 개발

SI 핵심 성능 분석 결과에 대한
Chart 생성 및 Reporting 자동화 시스템 개발

o 30GHz 대역 미세 배선의 고정밀/광대역 측정 기법 개발
: 2종 기법 병행 적용



EM simulation을 이용한 추정
: 공정 편차에 의한 오차 가능성

mTRL 기법에 의해 Calibration
: 측정 결과의 Zref(f)가 Line Z_0(f)로 설정됨
: Z_0(f)-> 50ohm Renormalization 필요

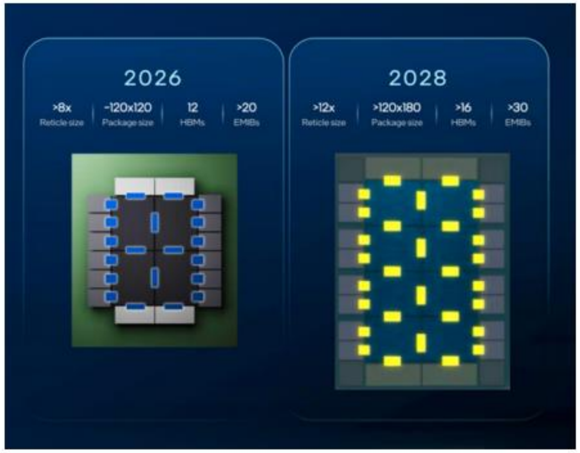
Calibration comparison 기법
: Error box를 circuit model로 근사화 하여 추정

전파 상수 기법
: mTRL로 얻은 Υ_{meas}를 기반으로
EM simulation 공정 오차 보정 -> $\Upsilon_{sim} \approx \Upsilon_{meas}$
: 보정된 EM simulation 결과로 부터 C 추정
: $Z_0 \approx \frac{\Upsilon_{sim}}{j\omega C}$

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 :

Packaging the AI Frontier: Intel Foundry’s Advanced Packaging Alignment with the XPU Industry Roadmap:

- ✓ 컴퓨팅 병목 현상 : AI 모델 연산량 대비 메모리와 인터커넥트 기술은 상대적으로 정체
- ✓ 패키징 중요성 증대 : 모놀리식 실리콘이 레티클 한계와 전력 밀도 문제 봉착 => 패키징 아키텍처가 AI 인프라 확장의 결정적 요소
- ✓ EMIB(Embedded Multi-Die Interconnect Bridge) : 실리콘 인터포저 대신 필요한 부분에만 실리콘 브릿지를 삽입하여 웨이퍼 활용도를 약 90%까지 높인 2.5D 통합 기술
- ✓ Foveros Direct 3D : 구리 대 구리 하이브리드 본딩을 통해 9마이크론 이하의 범프 피치 달성, 수직 적층 밀도 극대화
- ✓ 시스템 파운드리 모델 : 패키징 서비스를 제조 공정과 분리하여 제공, 고객사가 다양한 공정의 실리콘을 인텔의 패키징 기술로 통합할 수 있게 함.
- ✓ 2026년까지 12개 이상의 HBM 탑재, 2028년 레티클 크기의 12배에 달하는 대규모 슈퍼칩 패키징 지원



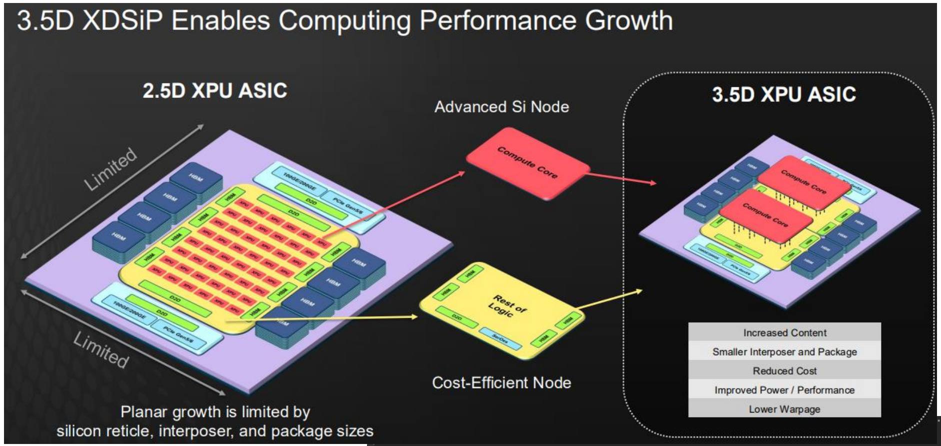
그림출처 :
https://futurumgroup.com/research-reports/packaging-the-ai-frontier-intel-foundrys-advanced-packaging-alignment-with-the-xpu-industry-roadmap/

[EMIB Scaling Roadmap, intel Foundry]

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 :

Enabling AI Infrastructure: 3.5D XDSiP^{TM} Platform Technology :

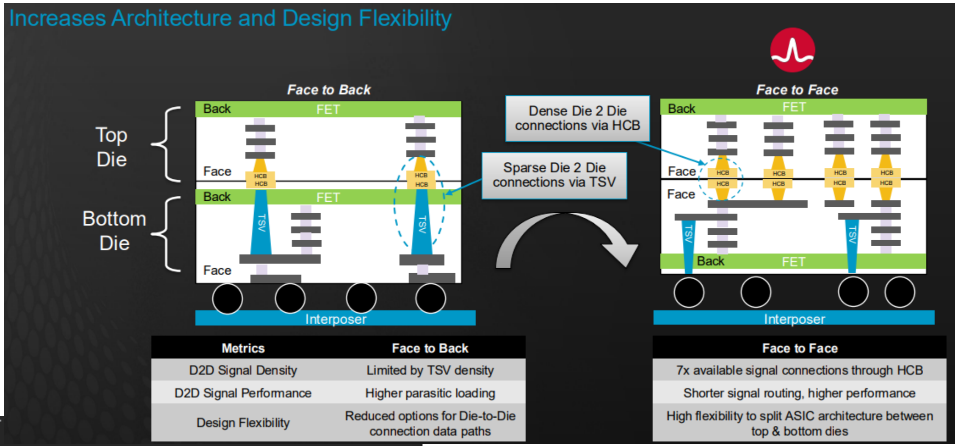
✓ Consumer –AI XPU Complexity and Performance Continuously Increasing



3.5D XDSiP Enables Computing Performance Growth

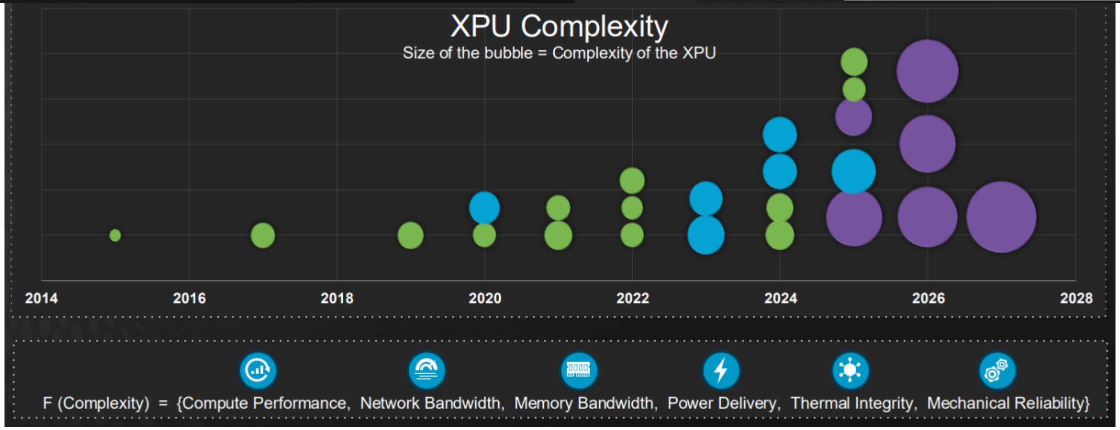
Increased Content
Smaller Interposer and Package
Reduced Cost
Improved Power / Performance
Lower Warpage

Planar growth is limited by
silicon reticle, interposer, and package sizes



Increases Architecture and Design Flexibility

Metrics	Face to Back	Face to Face
D2D Signal Density	Limited by TSV density	7x available signal connections through HCB
D2D Signal Performance	Higher parasitic loading	Shorter signal routing, higher performance
Design Flexibility	Reduced options for Die-to-Die connection data paths	High flexibility to split ASIC architecture between top & bottom dies



XPU Complexity

Size of the bubble = Complexity of the XPU

F (Complexity) = {Compute Performance, Network Bandwidth, Memory Bandwidth, Power Delivery, Thermal Integrity, Mechanical Reliability}

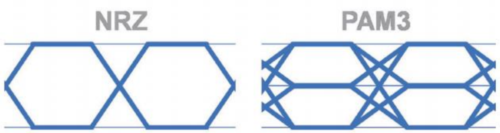
그림출처 : https://www.broadcom.com/info/ai/3point5d

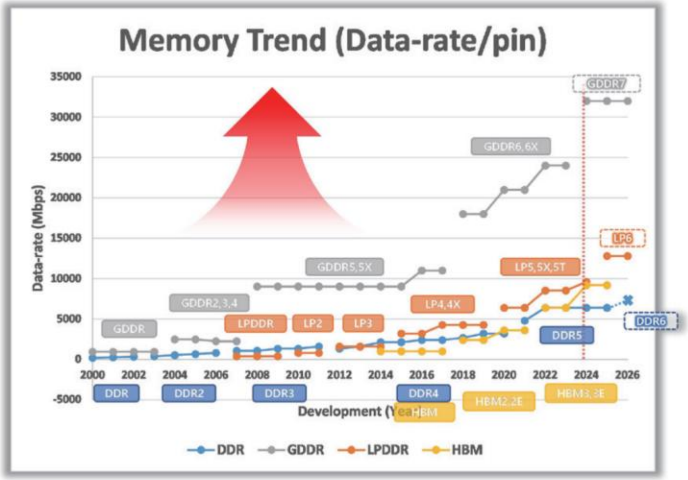
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 : 고속 대용량 메모리/SerDes 신호 전송을 위한 PCB 와 Interconnection 설계 시 발생하는 주요 이슈

High Speed / High Bandwidth / Low Voltage / Low Noise Margin

- GDDR6X : 24Gbps
- GDDR7 : 32Gbps PAM3, 32pin
- LPDDR5X : ~9.6Gbps, 32pin

  0.5V VDDQ
- HBM3E : ~9.8Gbps, 1024pin





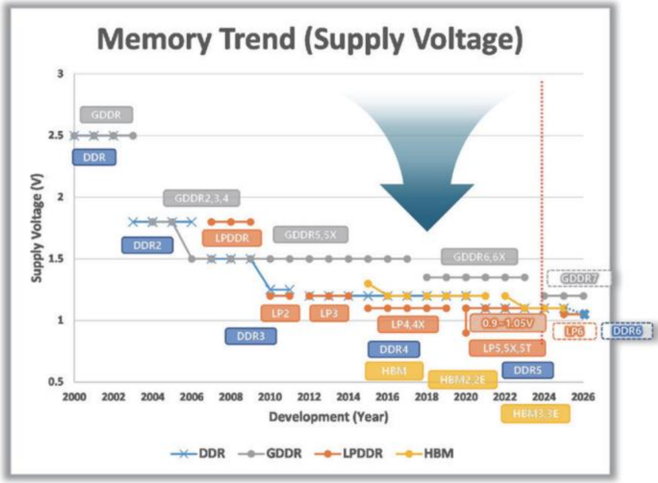
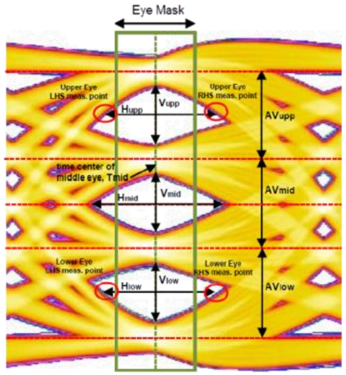


*그림 출처 : https://ettrends.etri.re.kr/ettrends/210/0905210015/

- PCIe Gen5 : 32GT/s NRZ , 32pair (16Lane Tx/Rx)
- PCIe Gen7 : 128GT/s PAM4



PAM4 signal Eye Parameters :

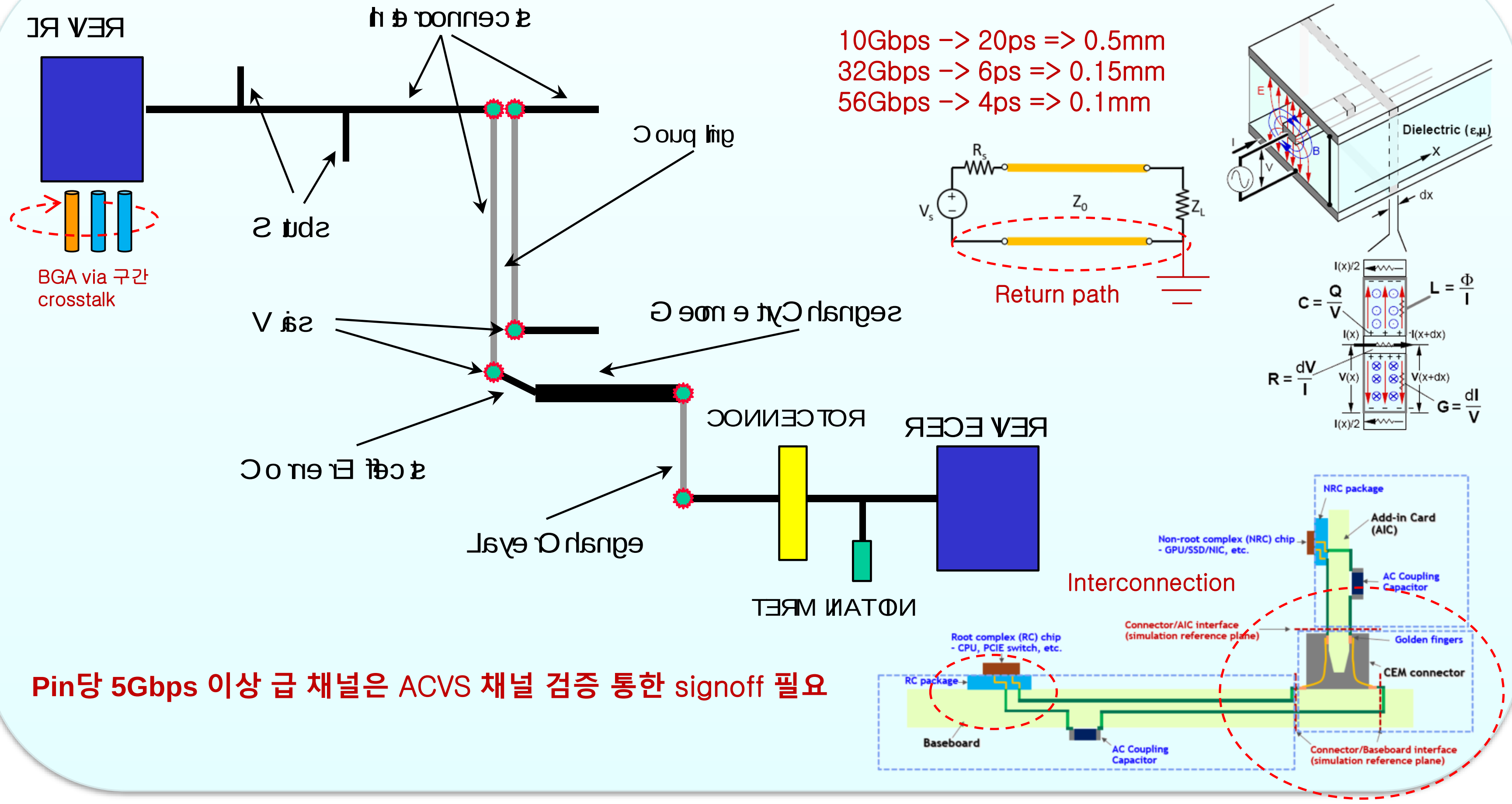
* PAM4의 경우 NRZ 대비 noise margin 이 30%이상 감소하므로, cross-talk, reflections, power noise 를 최소화 하도록 설계하여야 함.

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 : 고속 대용량 메모리/SerDes 신호 전송을 위한 PCB 와 Interconnection 설계 시 발생하는 주요 이슈

Signal Integrity / Return path / Interconnection Design

Trise : BW/5 => Z0 matching 이 필요해지는 거리

10Gbps -> 20ps => 0.5mm
32Gbps -> 6ps => 0.15mm
56Gbps -> 4ps => 0.1mm



- **Pin당 5Gbps 이상 급 채널은** ACVS **채널 검증 통한** signoff **필요**

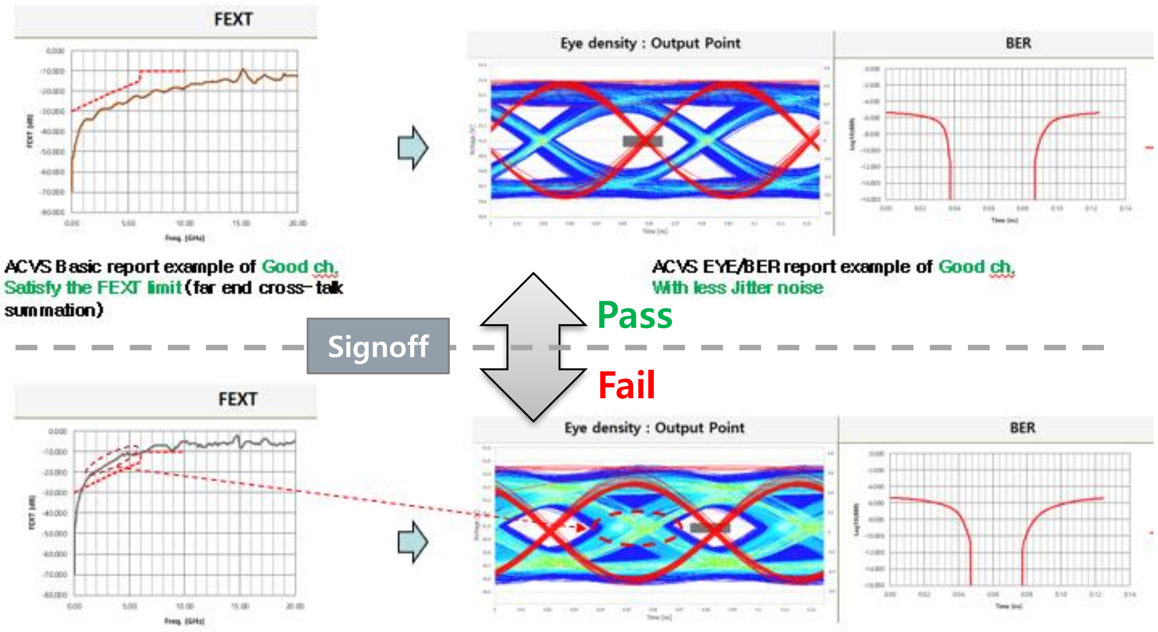
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 : 고속 대용량 메모리/SerDes 신호 전송을 위한 PCB 와 Interconnection 설계 시 발생하는 주요 이슈

Cross talk / Skew / ISI

NEXT limit :

PCIe Gen5	< −50dB
PCIe Gen6	< −62dB
112G Ethernet	< −65dB

➢ Huwin ACVS Basic SI (FEXT) and Eye/BER report results correlation example for Jitter analysis



ACVS Basic report example of Good ch. Satisfy the FEXT limit (far end cross-talk summation)

ACVS EYE/BER report example of Good ch. With less Jitter noise

Signoff

Pass

Fail

ACVS Basic report example of Bad ch. Over the FEXT limit (far end cross-talk summation)

ACVS EYE/BER report example of Bad ch. With more Jitter noise caused by FEXT

$$PSNEXT(f) = 20\log\left(\sum_n |NEXT\_n(f)|\right)$$

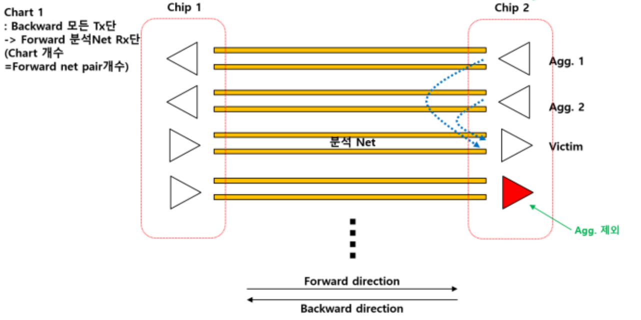


Chart 1
: Backward 모든 Tx단
-> Forward 분석Net Rx단
(Chart 개수
=Forward net pair개수)

$$PSFEXT(f) = 20\log\left(\sum_n |FEXT\_n(f)|\right)$$

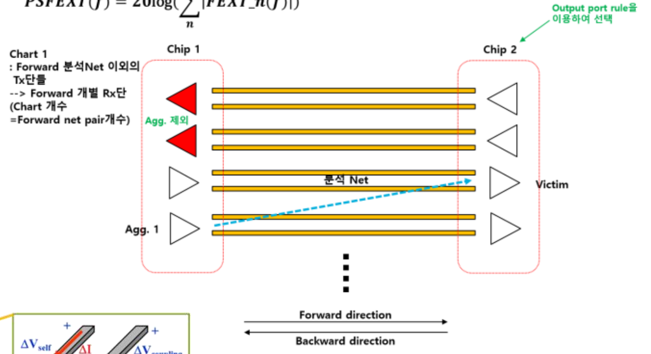
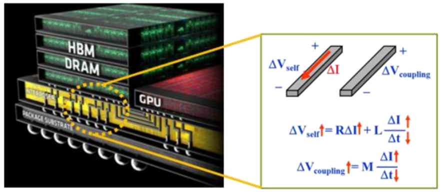


Chart 1
: Forward 분석Net 이외의 Tx단를
--> Forward 개별 Rx단
(Chart 개수
=Forward net pair개수)

- 대용량 및 고속 신호 전송에서 Crosstalk 이슈가 증가함.



$$\Delta V_{self}\uparrow = R\Delta I\uparrow + L\frac{\Delta I\uparrow}{\Delta t\downarrow}$$

$$\Delta V_{coupling}\uparrow = M\frac{\Delta I\uparrow}{\Delta t\downarrow}$$

- Smaller size & Narrower space

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 :

~ 250GHz : SPINNER Launches 0.5 mm Test Accessories for Ultra-High-Frequency Measurements up to 250 GHz

https://www.spinner-group.com/en/home/

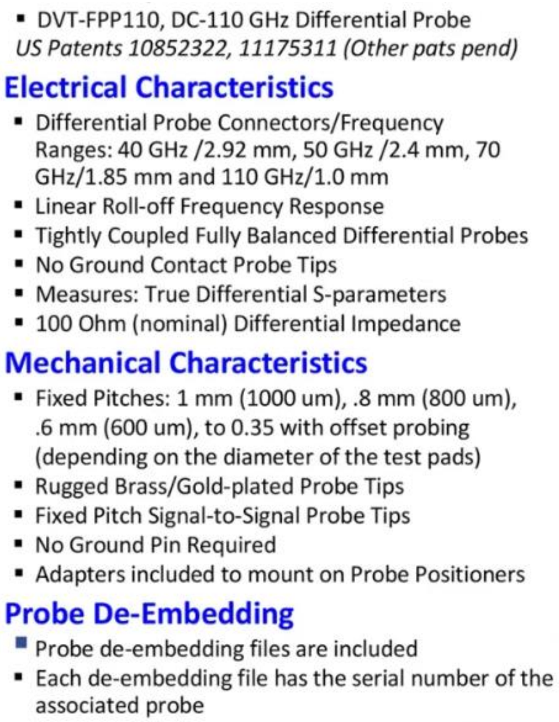
Waveguide-to-Coaxial Adapters

Board Connectivity

1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 :

Differential Wide Pitch Probing : Dual Differential Probing System

Enlarged side view of probe tips


- DVT-FPP110, DC-110 GHz Differential Probe

US Patents 10852322, 11175311 (Other pats pend)

Electrical Characteristics

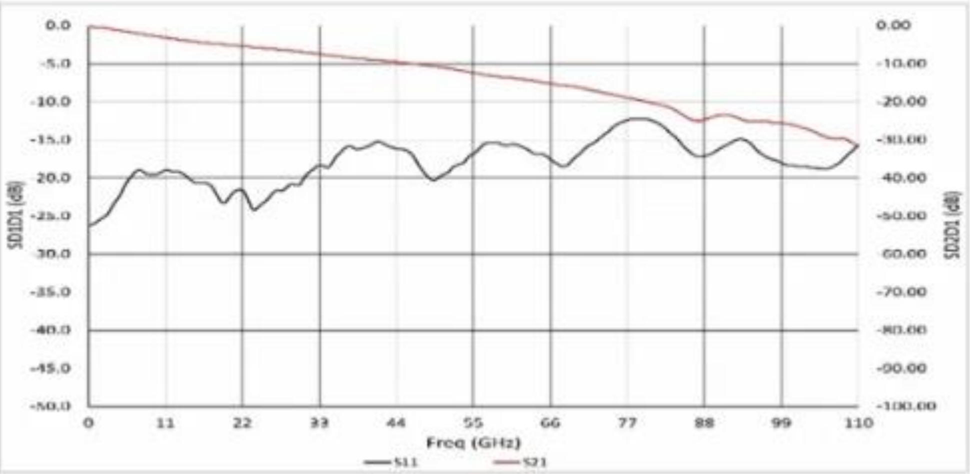
- Differential Probe Connectors/Frequency Ranges: 40 GHz /2.92 mm, 50 GHz /2.4 mm, 70 GHz/1.85 mm and 110 GHz/1.0 mm
- Linear Roll-off Frequency Response
- Tightly Coupled Fully Balanced Differential Probes
- No Ground Contact Probe Tips
- Measures: True Differential S-parameters
- 100 Ohm (nominal) Differential Impedance

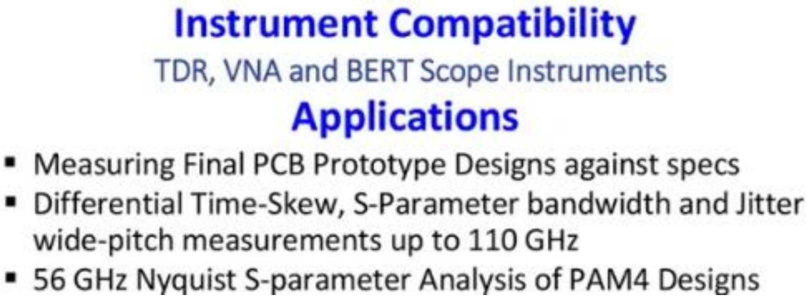
Mechanical Characteristics

- Fixed Pitches: 1 mm (1000 um), .8 mm (800 um), .6 mm (600 um), to 0.35 with offset probing (depending on the diameter of the test pads)
- Rugged Brass/Gold-plated Probe Tips
- Fixed Pitch Signal-to-Signal Probe Tips
- No Ground Pin Required
- Adapters included to mount on Probe Positioners

Probe De-Embedding

- Probe de-embedding files are included
- Each de-embedding file has the serial number of the associated probe




Instrument Compatibility

TDR, VNA and BERT Scope Instruments

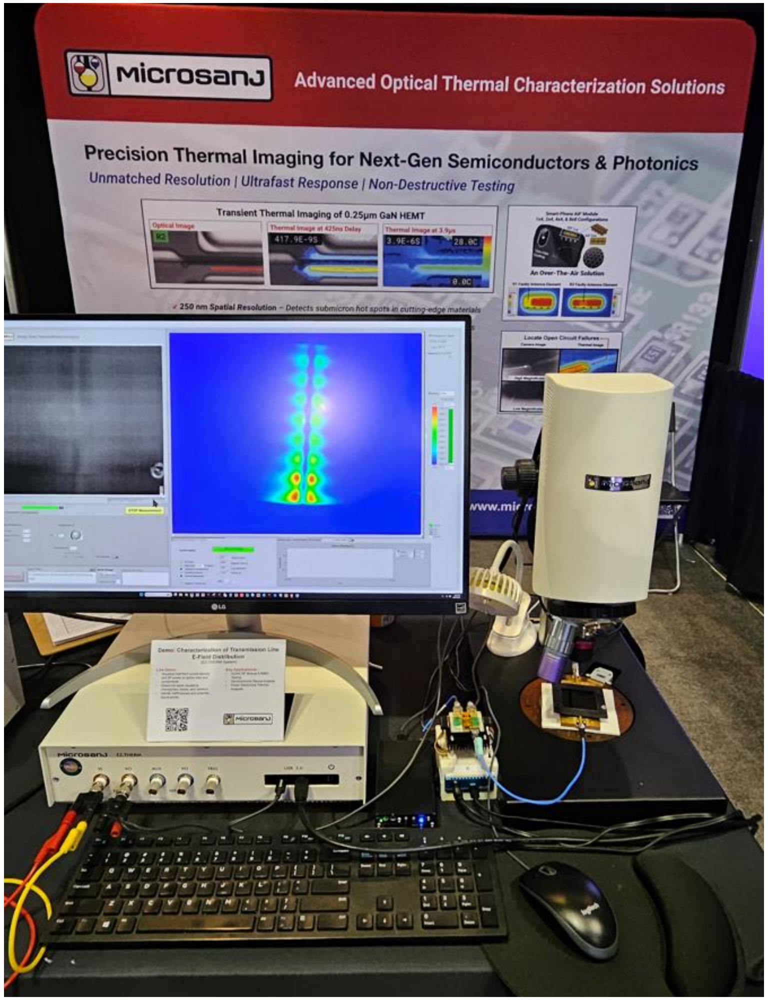
Applications

- Measuring Final PCB Prototype Designs against specs
- Differential Time-Skew, S-Parameter bandwidth and Jitter wide-pitch measurements up to 110 GHz
- 56 GHz Nyquist S-parameter Analysis of PAM4 Designs

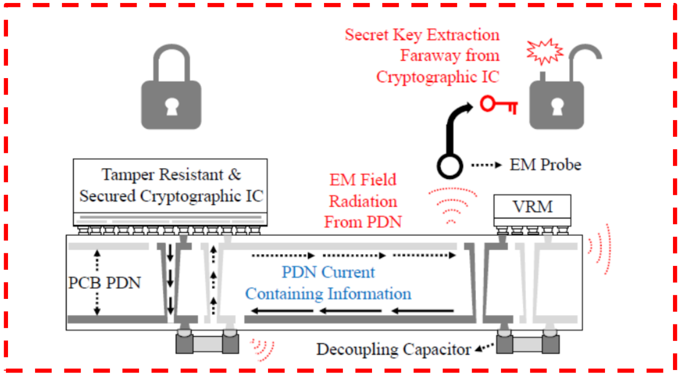
https://gigaprobes.com/

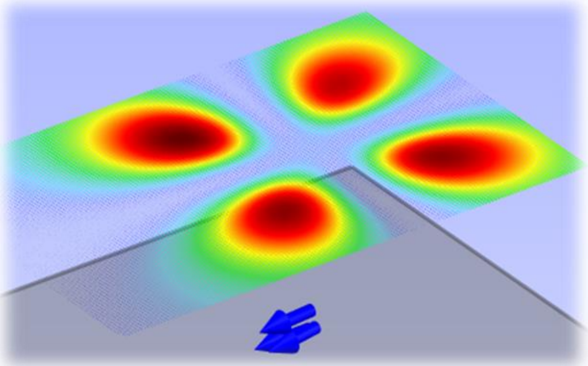
1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 :

Precision Thermal Imaging for Next-Gen Semiconductors & Photonics:



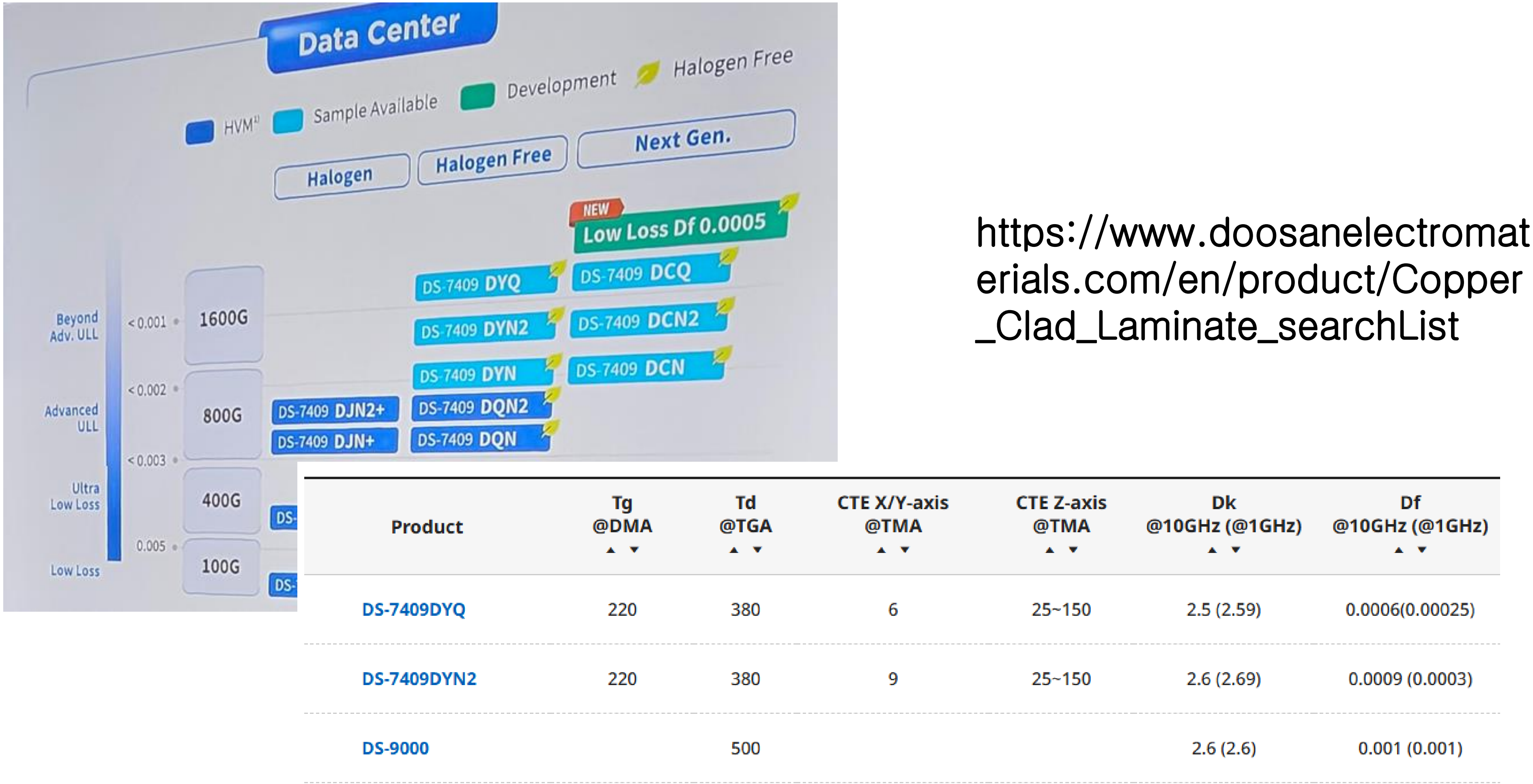
https://microsanj.com/products/thermoreflectance-imaging/sanjscope-ez500/





1. Advanced Silicon/Package/PCB SPGTI Design 기술동향 :

Low Loss Df 0.0005 :



Data Center

HVM¹⁾ Sample Available Development Halogen Free

Halogen | Halogen Free | Next Gen.

NEW Low Loss Df 0.0005

Beyond Adv. ULL < 0.001 1600G
DS-7409 DYQ
DS-7409 DCQ
DS-7409 DYN2
DS-7409 DCN2

Advanced ULL < 0.002 800G
DS-7409 DYN
DS-7409 DCN
DS-7409 DJN2+
DS-7409 DQN2
DS-7409 DJN+
DS-7409 DQN

Ultra Low Loss < 0.003 400G

Low Loss 0.005 100G

Product	Tg @DMA	Td @TGA	CTE X/Y-axis @TMA	CTE Z-axis @TMA	Dk @10GHz (@1GHz)	Df @10GHz (@1GHz)
DS-7409DYQ	220	380	6	25~150	2.5 (2.59)	0.0006(0.00025)
DS-7409DYN2	220	380	9	25~150	2.6 (2.69)	0.0009 (0.0003)
DS-9000		500			2.6 (2.6)	0.001 (0.001)

https://www.doosanelectromaterials.com/en/product/Copper_Clad_Laminate_searchList

목차

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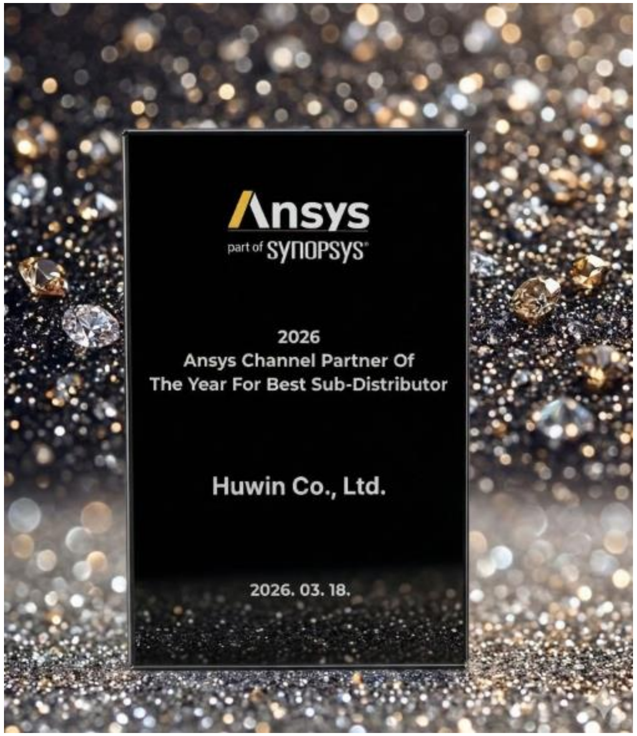
2. 시뮬레이션 통한 SPGTI 설계

3. DesignCon2026 자료 소개

Simulation
Next X



Ansys
part of synopsys

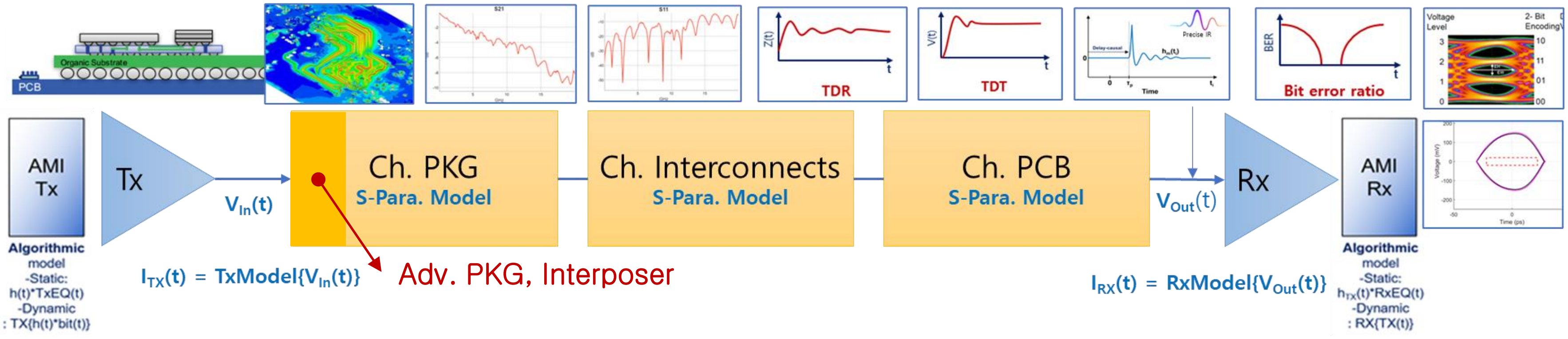
2026
Ansys Channel Partner Of
The Year For Best Sub-Distributor

Huwin Co., Ltd.

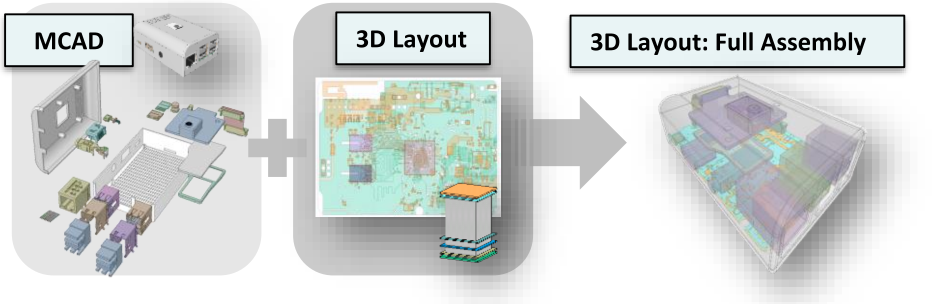
2026. 03. 18.

■ 2. 시뮬레이션 통한 SPGTI 설계 :

High Speed / High Bandwidth / Low Voltage / Low Noise Margin



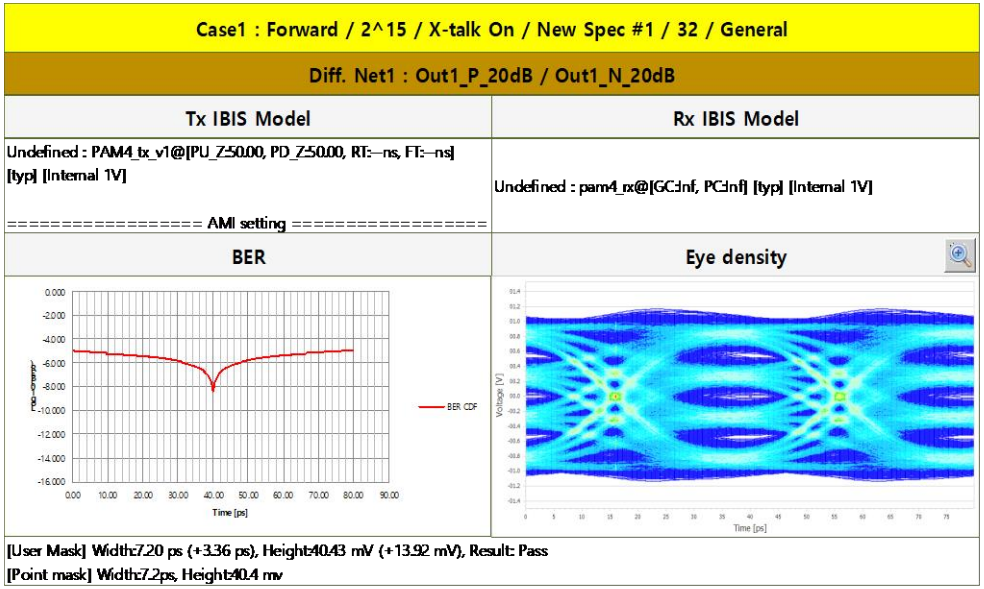
- Electronic System : High-speed, High-Bandwidth(density), Low Voltage(high current, high-power), Low noise margin
- 2023 : 800Gb(100G-PAM4 x 8lane) Ethernet , PCIe Gen6(PAM4), DDR5, GDDR6/7(PAM4)
- Copper Traces are lossy at high-speed
- Thermal Integrity
- Silicon Interposer (TSV)
- DC~140GHz S-parameters modeling => 3D EM modeling
- Accurate Impulse response from S-parameters
- Large number of ports (signals) ch. Models -> ~100GB
- AMI model for estimating BER/Eye Eye-diagram



Geometry changes can quickly be implemented, adaptive meshing gives confidence on every solution without user interaction

2. 시뮬레이션 통한 SPGTI 설계 :

Cross talk / Skew / ISI



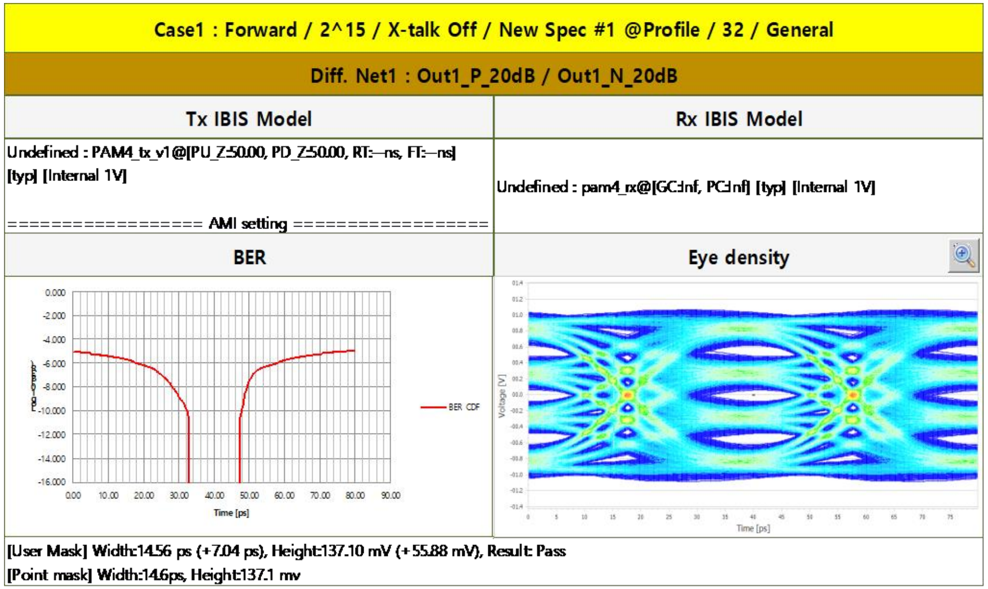
Case1 : Forward / 2^15 / X-talk On / New Spec #1 / 32 / General

Diff. Net1 : Out1_P_20dB / Out1_N_20dB

Tx IBIS Model	Rx IBIS Model
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ================== AMI setting ==================	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]

[User Mask] Width:7.20 ps (+3.36 ps), Height:40.43 mV (+13.92 mV), Result: Pass
[Point mask] Width:7.2ps, Height:40.4 mv

Xtalk를 반영한 eye 결과



Case1 : Forward / 2^15 / X-talk Off / New Spec #1 @Profile / 32 / General

Diff. Net1 : Out1_P_20dB / Out1_N_20dB

Tx IBIS Model	Rx IBIS Model
Undefined : PAM4_tx_v1@[PU_Z:50.00, PD_Z:50.00, RT:--ns, FT:--ns] [typ] [Internal 1V] ================== AMI setting ==================	Undefined : pam4_rx@[GC:Inf, PC:Inf] [typ] [Internal 1V]

[User Mask] Width:14.56 ps (+7.04 ps), Height:137.10 mV (+55.88 mV), Result: Pass
[Point mask] Width:14.6ps, Height:137.1 mv

Xtalk를 반영하지 않은 eye 결과

Fail ⇔ 🚫

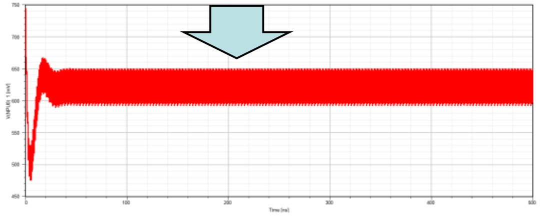
Signoff

- 대용량 및 고속 신호 전송에서 Crosstalk 이슈가 증가함.

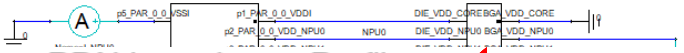
2. 시뮬레이션 통한 SPGTI 설계 :

CPM/DIE decoupling circuit + PDN model -> AC ripple (transient) Simulation

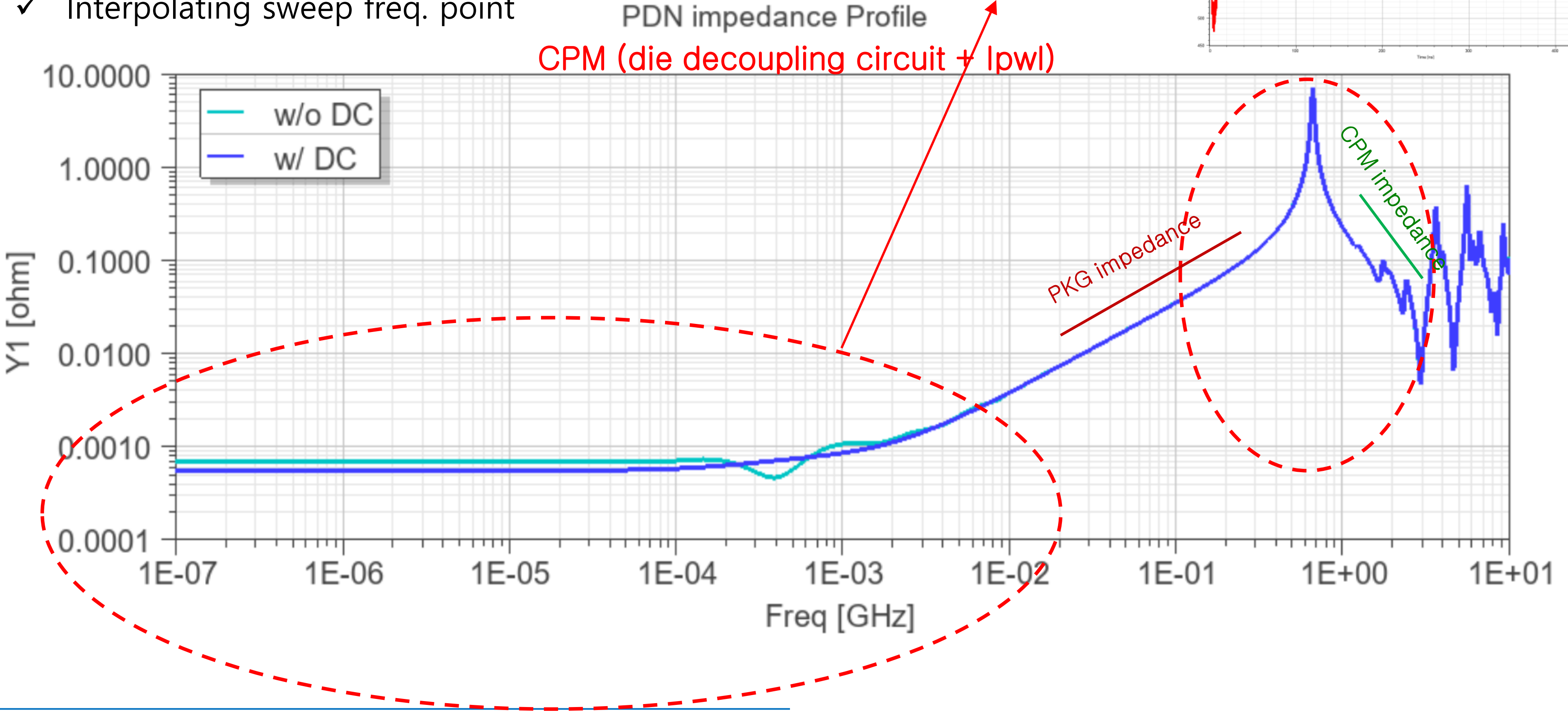
- ✓ Transient 분석 위한 PDN model 추출 : Port Impedance/renormalize, Low Freq. Sweep, Capacitor model
- ✓ Interposer model 추출 : mesh resolution
- ✓ 추출 Ipwl 모델 spectrum 검증(Tstop, Tstep)
- ✓ Exact DC 추출
- ✓ Interpolating sweep freq. point



PDN



CPM (die decoupling circuit + Ipwl)

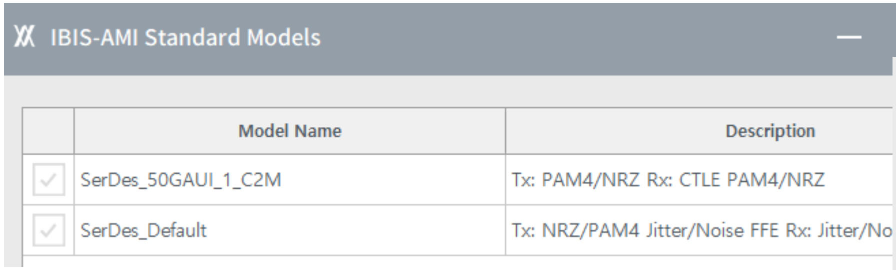


2. 시뮬레이션 통한 SPGTI 설계 :

Standard Library & Spec.

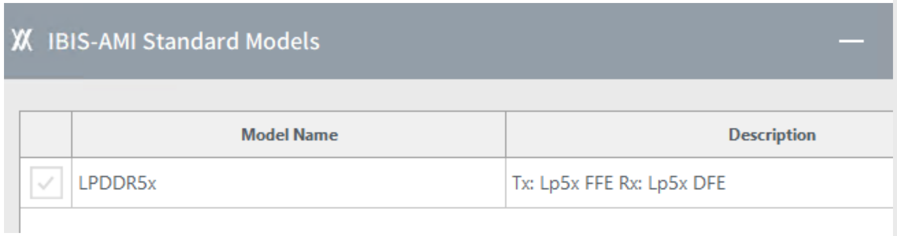
- ✓ 채널별 Basic SI Limit
- ✓ Interface 별 Standard IO model Library
  => SerDes, LPDDR5x 등
- ✓ OIF CEI 규격별 Eye Mask Spec
- ✓ UCIe VTF Standard setup 등

Standard Models



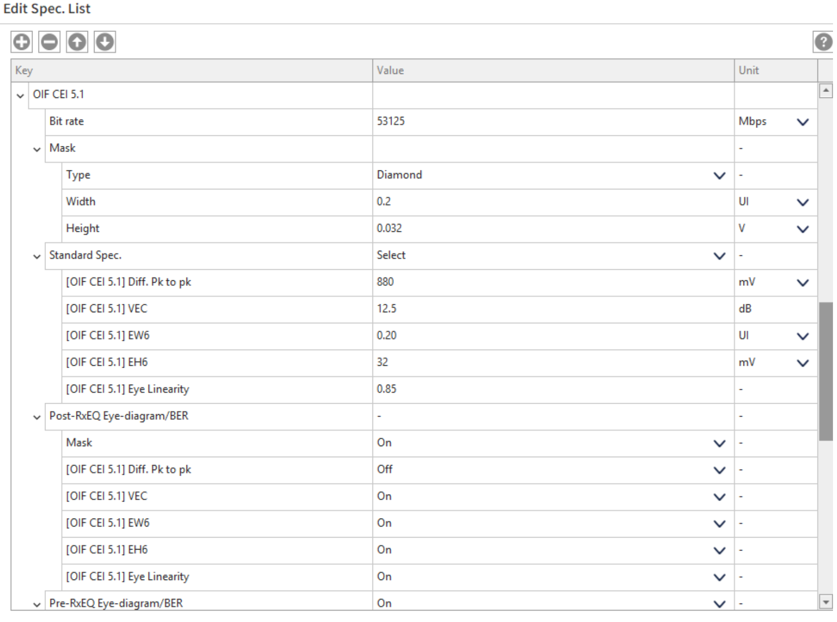
	Model Name	Description
✓	SerDes_50GAUI_1_C2M	Tx: PAM4/NRZ Rx: CTLE PAM4/NRZ
✓	SerDes_Default	Tx: NRZ/PAM4 Jitter/Noise FFE Rx: Jitter/No

…

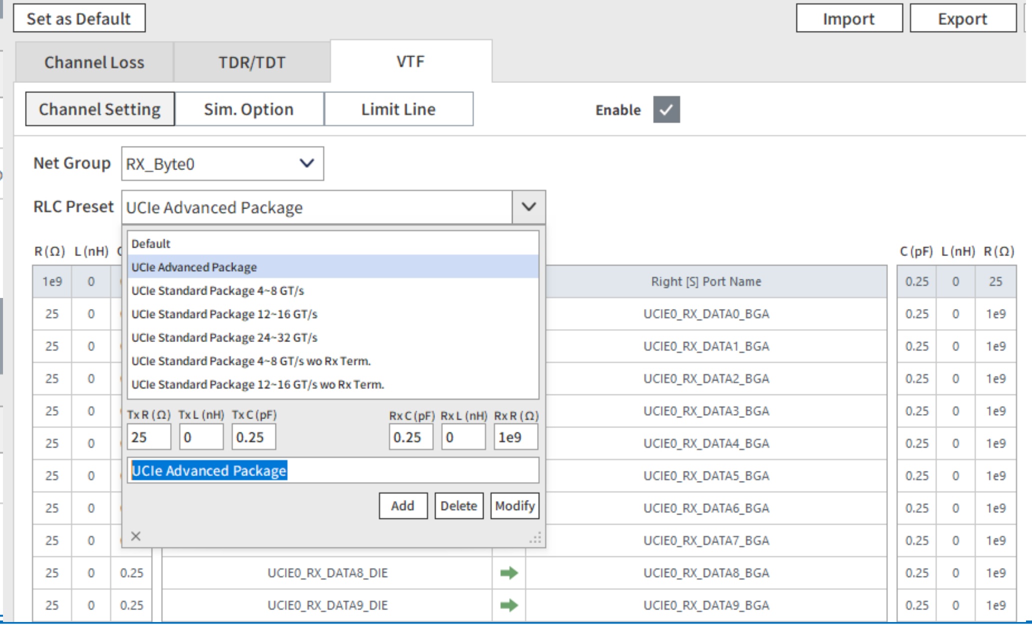


	Model Name	Description
✓	LPDDR5x	Tx: Lp5x FFE Rx: Lp5x DFE

…



Key	Value	Unit
OIF CEI 5.1		
Bit rate	53125	Mbps
Mask		-
Type	Diamond	-
Width	0.2	UI
Height	0.032	V
Standard Spec.	Select	-
[OIF CEI 5.1] Diff. Pk to pk	880	mV
[OIF CEI 5.1] VEC	12.5	dB
[OIF CEI 5.1] EW6	0.20	UI
[OIF CEI 5.1] EH6	32	mV
[OIF CEI 5.1] Eye Linearity	0.85	-
Post-RxEQ Eye-diagram/BER	-	-
Mask	On	-
[OIF CEI 5.1] Diff. Pk to pk	Off	-
[OIF CEI 5.1] VEC	On	-
[OIF CEI 5.1] EW6	On	-
[OIF CEI 5.1] EH6	On	-
[OIF CEI 5.1] Eye Linearity	On	-
Pre-RxEQ Eye-diagram/BER	On	-



Enable ☑

Net Group: RX_Byte0

RLC Preset: UCIe Advanced Package

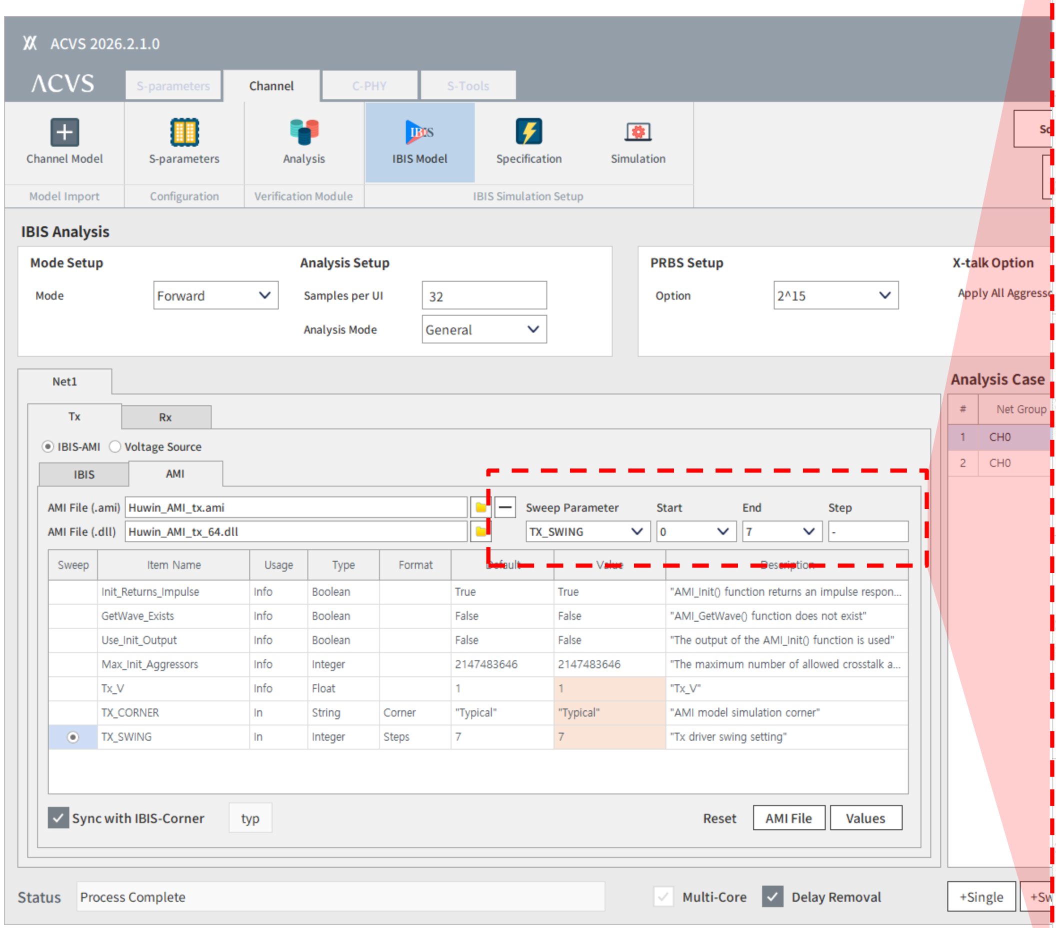
Tx R (Ω): 25 Tx L (nH): 0 Tx C (pF): 0.25 Rx C (pF): 0.25 Rx L (nH): 0 Rx R (Ω): 1e9

UCIe Advanced Package

R (Ω)	L (nH)	C			Right [S] Port Name	C (pF)	L (nH)	R (Ω)
1e9	0					0.25	0	25
25	0				UCIE0_RX_DATA0_BGA	0.25	0	1e9
25	0				UCIE0_RX_DATA1_BGA	0.25	0	1e9
25	0				UCIE0_RX_DATA2_BGA	0.25	0	1e9
25	0				UCIE0_RX_DATA3_BGA	0.25	0	1e9
25	0				UCIE0_RX_DATA4_BGA	0.25	0	1e9
25	0				UCIE0_RX_DATA5_BGA	0.25	0	1e9
25	0				UCIE0_RX_DATA6_BGA	0.25	0	1e9
25	0				UCIE0_RX_DATA7_BGA	0.25	0	1e9
25	0	0.25	UCIE0_RX_DATA8_DIE	➡	UCIE0_RX_DATA8_BGA	0.25	0	1e9
25	0	0.25	UCIE0_RX_DATA9_DIE	➡	UCIE0_RX_DATA9_BGA	0.25	0	1e9

2. 시뮬레이션 통한 SPGTI 설계 :

AMI Parameter Sweep



IBIS Analysis

Mode Setup

Mode: Forward

Analysis Setup

Samples per UI: 32

Analysis Mode: General

PRBS Setup

Option: 2^15

X-talk Option

Apply All Aggress

Analysis Case

#	Net Group
1	CH0
2	CH0

● IBIS-AMI ○ Voltage Source

AMI File (.ami): Huwin_AMI_tx.ami

AMI File (.dll): Huwin_AMI_tx_64.dll

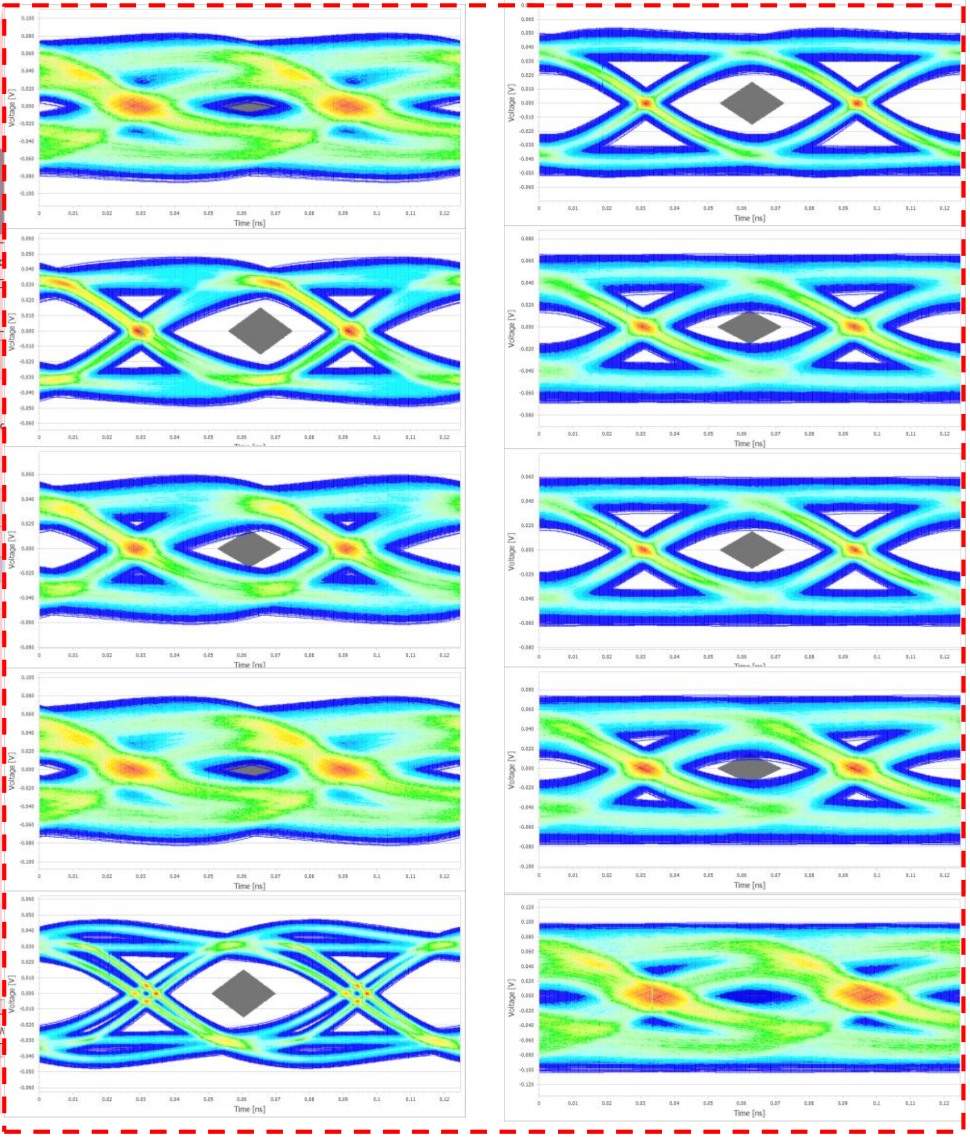
Sweep Parameter	Start	End	Step
TX_SWING	0	7	-

Sweep	Item Name	Usage	Type	Format	Default	Value	Description
	Init_Returns_Impulse	Info	Boolean		True	True	"AMI_Init() function returns an impulse respon...
	GetWave_Exists	Info	Boolean		False	False	"AMI_GetWave() function does not exist"
	Use_Init_Output	Info	Boolean		False	False	"The output of the AMI_Init() function is used"
	Max_Init_Aggressors	Info	Integer		2147483646	2147483646	"The maximum number of allowed crosstalk a...
	Tx_V	Info	Float		1	1	"Tx_V"
	TX_CORNER	In	String	Corner	"Typical"	"Typical"	"AMI model simulation corner"
●	TX_SWING	In	Integer	Steps	7	7	"Tx driver swing setting"

☑ Sync with IBIS-Corner: typ

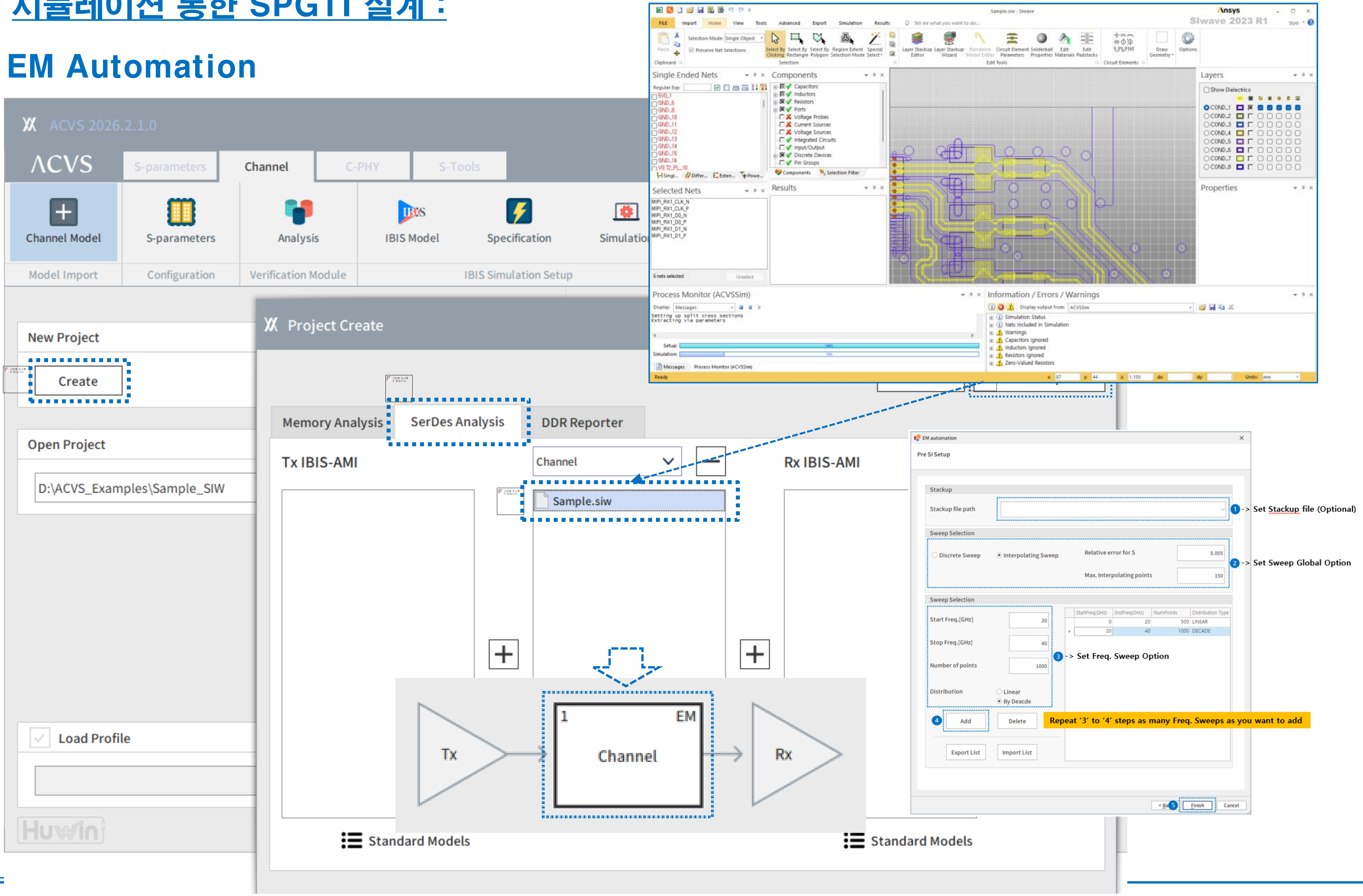
Status: Process Complete

☐ Multi-Core ☑ Delay Removal



2. 시뮬레이션 통한 SPGTI 설계 :

EM Automation



D:\ACVS_Examples\Sample_SIW

Channel

Sample.siw

1

Selected Nets:
- MIPI_RX1_CLK_N
- MIPI_RX1_CLK_P
- MIPI_RX1_D0_N
- MIPI_RX1_D0_P
- MIPI_RX1_D1_N
- MIPI_RX1_D1_P

```
Setting up split cross sections
Extracting via parameters
```

EM automation — Pre SI Setup

Stackup

Stackup file path: (empty)

① -> Set Stackup file (Optional)

Sweep Selection

○ Discrete Sweep ● Interpolating Sweep

Relative error for S: 0.005

Max. Interpolating points: 150

② -> Set Sweep Global Option

Sweep Selection

Start Freq.[GHz]: 20

Stop Freq.[GHz]: 40

Number of points: 1000

Distribution: ○ Linear ● By Deacde

StartFreq(GHz)	EndFreq(GHz)	NumPoints	Distribution Type
0	20	500	LINEAR
20	40	1000	DECADE

③ -> Set Freq. Sweep Option

④ Add

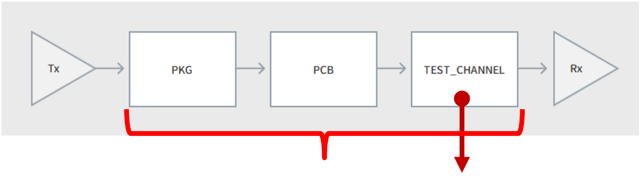
Repeat '3' to '4' steps as many Freq. Sweeps as you want to add

⑤ Finish

2. 시뮬레이션 통한 SPGTI 설계 :

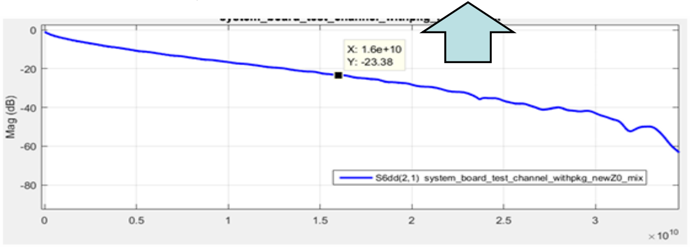
PCIe Gen6 PRBS20 분석

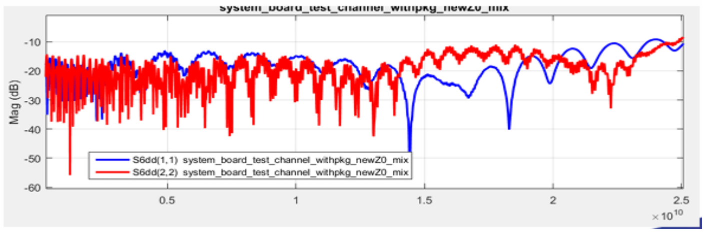
- ✓ Eye 분석 위한 Signal model 추출 : interpolation (x) , x-talk limit (<-60dB)
- ✓ PAM4 BER check => Error counts < 30 for 1M symbols simulation (excluding ignored bits)
  => Ignored bit ~ 3,200,000 bits + PRBS20 (1,048,575 bits)
  => ACVS 분석 시간 : 16 Ch., Crosstalk 포함 => 13시간 (multi core 적용 x) → ~2시간 (multi core 적용)
- ✓ Simulation symbols to 1e6 and target BER to 1e-6 => FEC 고려하면 1e-12 수준

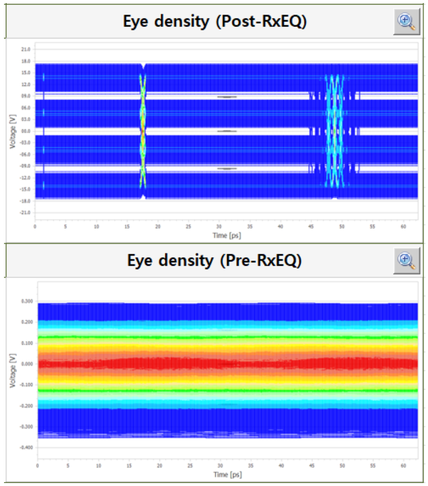


−32 @16GHz
Compliance 조건

−23.5dB @16GHz
Loss model

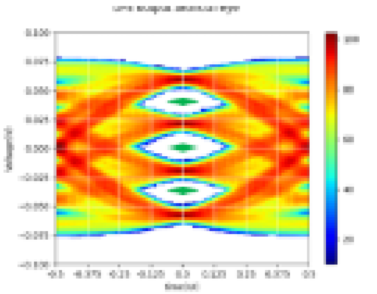


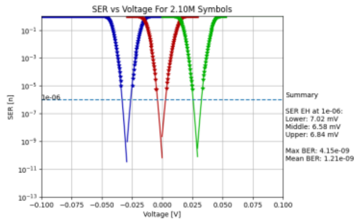




*.bin

IP업체 Post tool





Summary

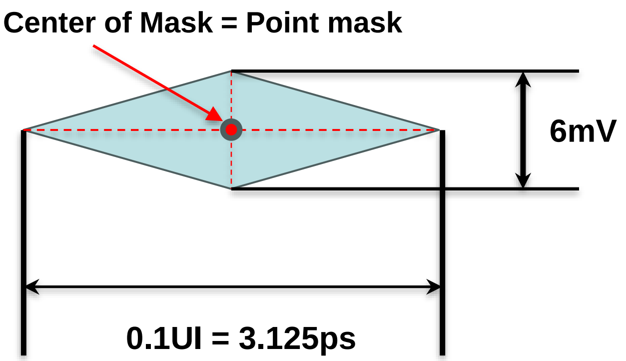
SER EH at 1e-06:
Lower: 7.02 mV
Middle: 6.58 mV
Upper: 6.84 mV

Max BER: 4.15e-09
Mean BER: 1.21e-09

2. 시뮬레이션 통한 SPGTI 설계 :

PAM4, Eye Measure

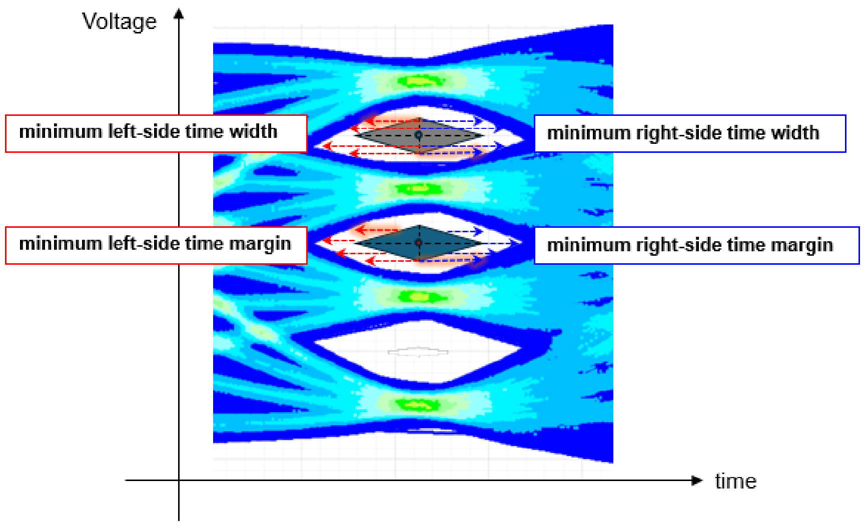
PCIe Gen6 Rx Mask Spec.



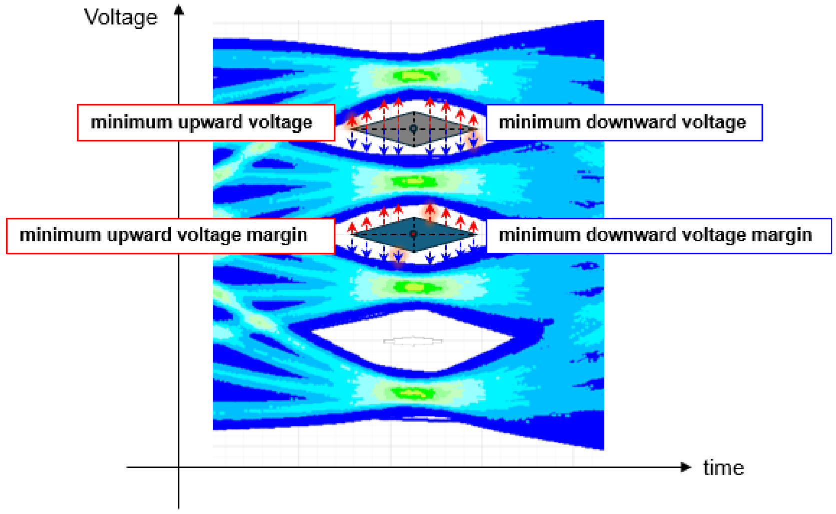
***PCIe Gen6 64GT/s (PAM4, 32 Gbaud)**
1 UI = 1 / 32 x 10^9 = 31.25ps

ACVS PAM4 Eye measure

Eye width margin (ps) = minimum left-side time margin + minimum right-side time margin
Eye width (ps) = minimum left-side time width + minimum right-side time width



Eye Height margin (V) = minimum upward voltage margin + minimum downward voltage margin
Eye Height (V) = minimum upward voltage + minimum downward voltage



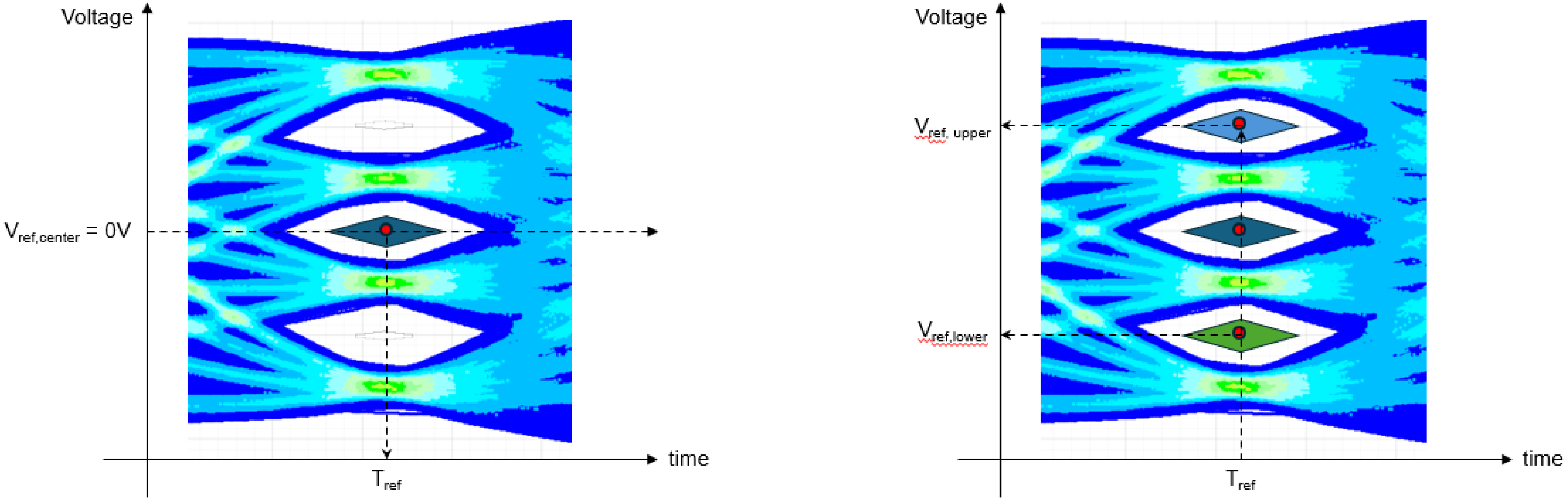
2. 시뮬레이션 통한 SPGTI 설계 :

PAM4, Eye Measure

Mask placement step

(1) 가운데 Eye(center eye)를 기준으로 $V_{ref,center}$ = 0V, Tref 선정
→ Eye opening이 최대가 되는 지점 탐색

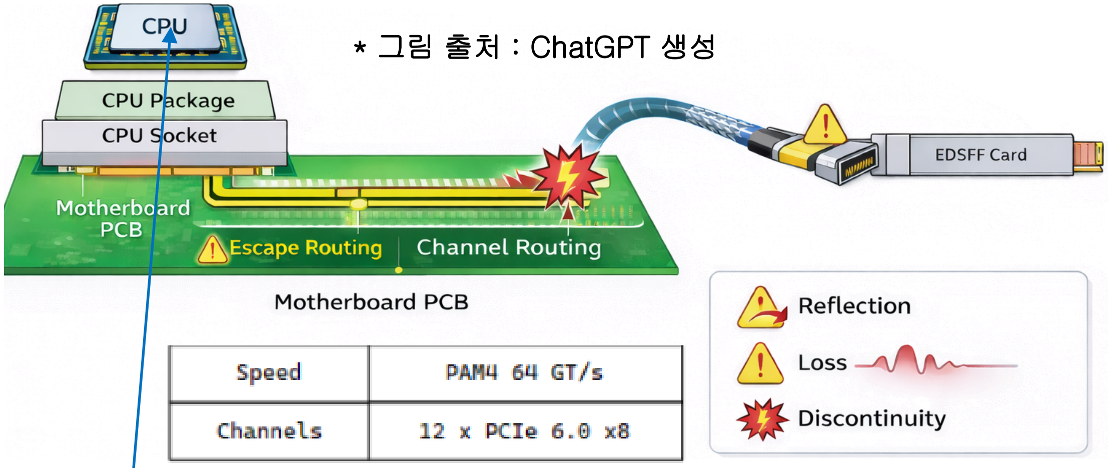
(2) Tref 기준으로 $V_{ref,upper}$, $V_{ref,lower}$ 선정 (T_{ref} 는 upper, center, lower 모두 공통)
→ 각 eye height가 최대가 되는 지점 탐색



ACVS PAM4 Eye measure

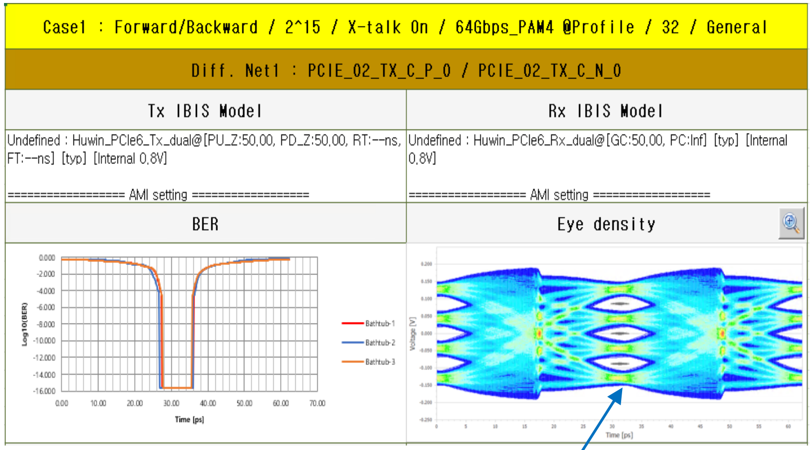
2. 시뮬레이션 통한 SPGTI 설계 :

EDSFF : "엔터프라이즈 및 데이터센터 표준 폼 팩터"

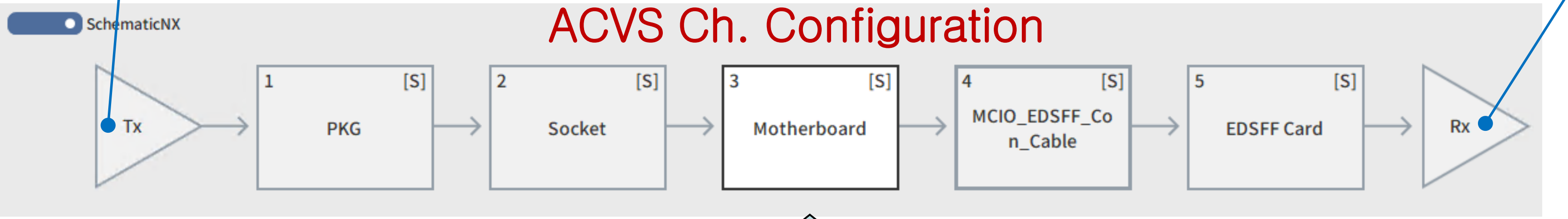


* 그림 출처 : ChatGPT 생성

Speed	PAM4 64 GT/s
Channels	12 x PCIe 6.0 x8



Case1 : Forward/Backward / 2^15 / X-talk On / 64Gbps_PAM4 @Profile / 32 / General	
Diff. Net1 : PCIE_02_TX_C_P_0 / PCIE_02_TX_C_N_0	
Tx IBIS Model	Rx IBIS Model
Undefined : Huwin_PCIe6_Tx_dual@[PU_Z:50,00, PD_Z:50,00, RT:--ns, FT:--ns] [typ] [Internal 0,8V] ================== AMI setting ==================	Undefined : Huwin_PCIe6_Rx_dual@[GC:50,00, PC:Inf] [typ] [Internal 0,8V] ================== AMI setting ==================
BER	Eye density



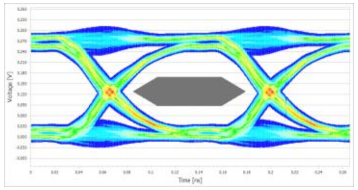
ACVS Ch. Configuration

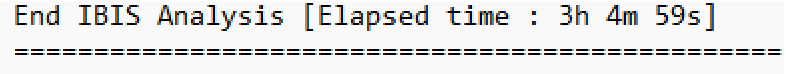
*.s384p : diff 96ch. (48lane)

2. 시뮬레이션 통한 SPGTI 설계 :

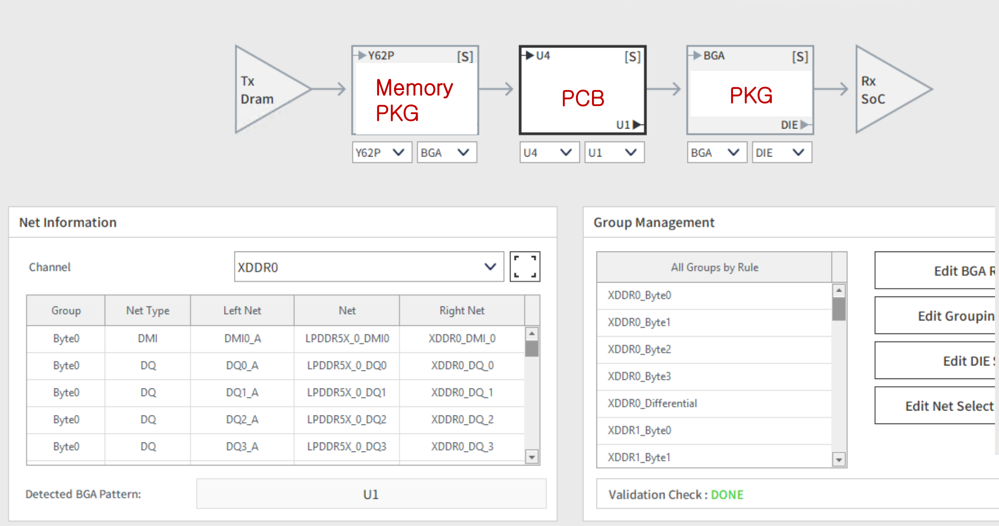
Memory 1100 포트 이상 채널

- ✓ # of ports : 1112 , ~20GHz, 25.7GB file size
- ✓ PRBS15(2^15) bit full transient analysis (32,767 bits)
- ✓ Memory : IBIS AMI Rx model
- ✓ Analysis time : 3h. 5m.





```
End IBIS Analysis [Elapsed time : 3h 4m 59s]
================================================
```



Net Information

Channel: XDDR0

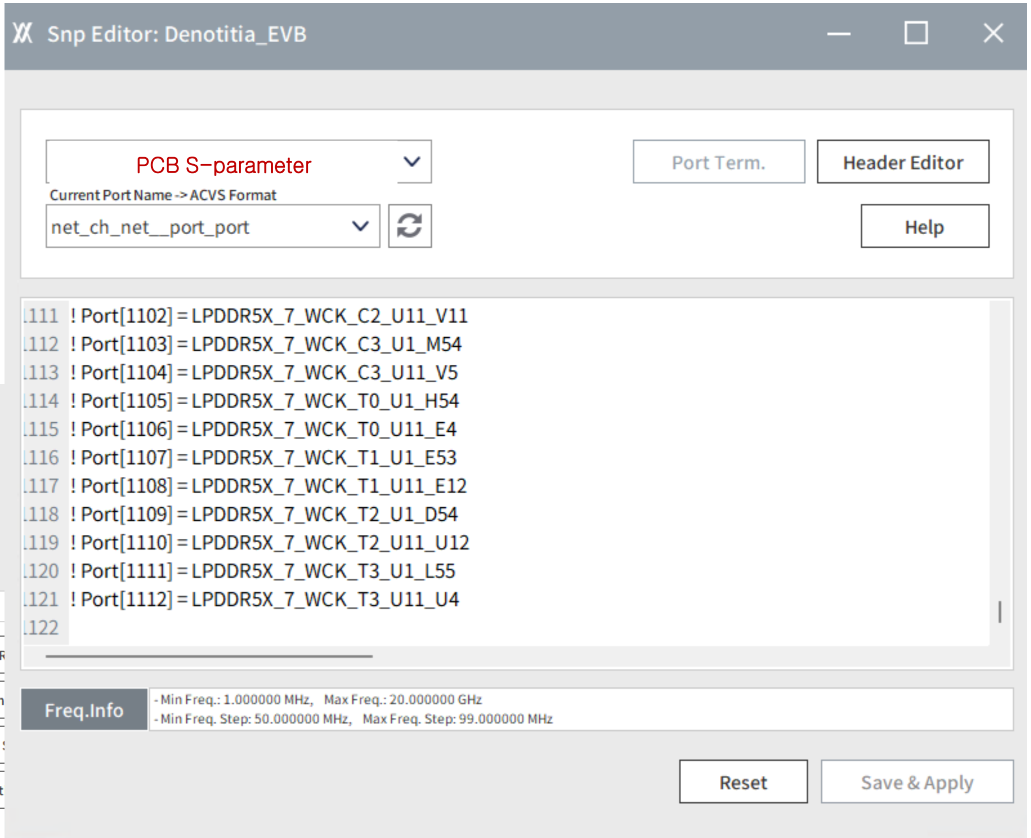
Group	Net Type	Left Net	Net	Right Net
Byte0	DMI	DMI0_A	LPDDR5X_0_DMI0	XDDR0_DMI_0
Byte0	DQ	DQ0_A	LPDDR5X_0_DQ0	XDDR0_DQ_0
Byte0	DQ	DQ1_A	LPDDR5X_0_DQ1	XDDR0_DQ_1
Byte0	DQ	DQ2_A	LPDDR5X_0_DQ2	XDDR0_DQ_2
Byte0	DQ	DQ3_A	LPDDR5X_0_DQ3	XDDR0_DQ_3

Detected BGA Pattern: U1

Group Management

All Groups by Rule
XDDR0_Byte0
XDDR0_Byte1
XDDR0_Byte2
XDDR0_Byte3
XDDR0_Differential
XDDR1_Byte0
XDDR1_Byte1

Validation Check : DONE



PCB S−parameter

Current Port Name -> ACVS Format: net_ch_net__port_port

```
! Port[1102] = LPDDR5X_7_WCK_C2_U11_V11
! Port[1103] = LPDDR5X_7_WCK_C3_U1_M54
! Port[1104] = LPDDR5X_7_WCK_C3_U11_V5
! Port[1105] = LPDDR5X_7_WCK_T0_U1_H54
! Port[1106] = LPDDR5X_7_WCK_T0_U11_E4
! Port[1107] = LPDDR5X_7_WCK_T1_U1_E53
! Port[1108] = LPDDR5X_7_WCK_T1_U11_E12
! Port[1109] = LPDDR5X_7_WCK_T2_U1_D54
! Port[1110] = LPDDR5X_7_WCK_T2_U11_U12
! Port[1111] = LPDDR5X_7_WCK_T3_U1_L55
! Port[1112] = LPDDR5X_7_WCK_T3_U11_U4
```

- Min Freq.: 1.000000 MHz, Max Freq.: 20.000000 GHz
- Min Freq. Step: 50.000000 MHz, Max Freq. Step: 99.000000 MHz

ACVS 이용한 고속 대용량 신호 PCB 와 Interconnection 설계 검증 Flow 소개

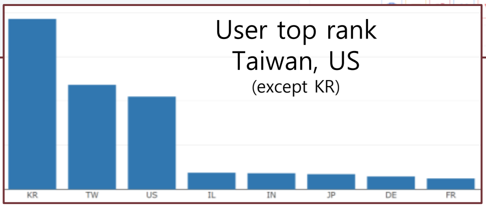
2. 시뮬레이션 통한 SPGTI 설계 :

SnpView.com

A High-Value, Professional Signal Integrity Simulator—Free to Use Online

- Basic charts: dB/phase, real/img, smith chart, group delay, passivity
- Advanced charts: **TDR, TDT, Eye-diagram (w. EQ, Jitter, Noise)**
- Advanced functions: **PerfectCal®** (lite), Snp Heal
- Powered by **SimNX**

Bit rate 10 Gbps
PRBS 30000 bits
IgnoreBits 1000 bits
Modulation ○ NRZ ● PAM4
Gray coding ● Off ○ On
Mask ○ On ○ Off
Mask width1 0.3 UI
Mask width2 0.5 UI
Mask width3 10 mV


User top rank
Taiwan, US
(except KR)


Visitors
✓ **500~1000/**day

Powered by SimNX